Monolithic CMOS Pixel Detector for ILC Vertex Detection

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Abstract. A monolithic CMS pixel detector is under development for an ILC experiment. This Chronopixel array provides a time stamp resolution of one bunch crossing, a critical feature for background suppression. The status of this effort is summarized.

1. Introduction

Studies in the U.S., Europe, and Asia, have demonstrated the power of a pixel vertex detector in experiments at a future high energy linear collider. Silicon CCDs (Charged Coupled Devices) [1] seemed like the vertex detector sensors of choice for the International Linear Collider (ILC) until the accelerator technology decision. With the choice of a cold TESLA-like superconducting technology for the ILC's main accelerator, the usefulness of CCDs for vertex detection is problematical. The time structure of this cold technology necessitates an extremely fast readout of the vertex detector elements and thus existing CCDs are not adequate. New CCD architectures are under development [2] but have yet to achieve the required performance. For these reasons there is an increased importance on the development of monolithic CMOS pixel detectors that allow extremely fast non-sequential readout of only hit pixels. This feature significantly decreases the readout time required. Last year, recognizing the potential of a monolithic CMOS detector, we initiated an R&D effort to develop such devices. [3] Our conceptual design for these CMOS detectors generates a time stamp on each hit with single bunch crossing precision. These "Chronopixel" detectors thereby significantly reduce the effective backgrounds relative to a sensor that integrates over many bunch crossings.
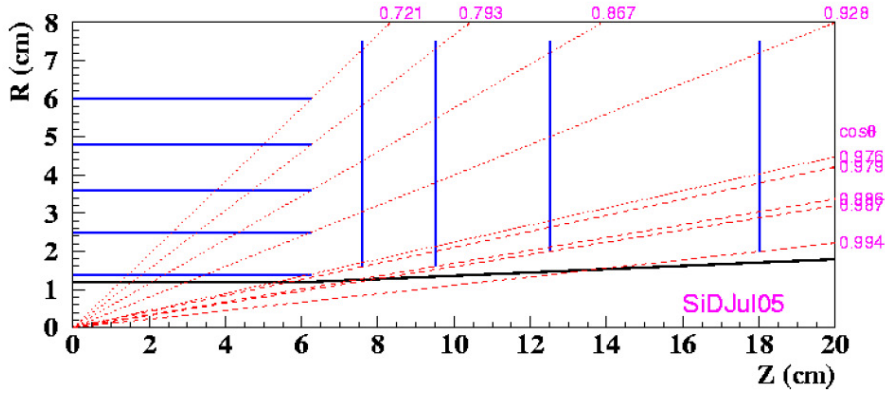
Figure 1. SiD Vertex Detector Configuration

2. Straw Man Vertex Detector Design

The overall vertex detector design of SiD is shown in Figure 1, and the numbers and sizes of the 292 detector elements (chips) are summarized in Tables 1 and 2.

Table 1. CMOS Detector Barrel Configuration

Layer	Radius (cm)	Total Length(cm)	No of Chips	Chip Size(cm^2)
1	1.4	12.5	12	12.5×1.2
2	2.5	12.5	24	12.5×1.2
3	3.6	12.5	20	12.5×2.2
4	4.8	12.5	20	12.5×2.2
5	6.0	12.5	24	12.5×2.2

Table 2. CMOS Detector Forward Disk Configuration

Annulus	Inner Radius(cm)	Z(cm)	No. of Chips	Chip Size(cm^2)
1	1.6	7.6	24	1.5×0.9
	3.1	7.6	24	4.4×2.2
2	1.6	9.5	24	1.5×0.9
	3.1	9.5	24	4.4×2.2
3	2.0	12.5	24	1.1×0.9
	3.1	12.5	24	4.4×2.2
4	2.0	18.0	24	1.1×0.9
	3.1	18.0	24	4.4×2.2

The baseline time structure of the ILC results from bunchtrains of 2820 bunches spaced 337 nanoseconds, passing through the collider hall 5 times a second. Consequently, each bunch train is about 1 msec long, with about 200 msec between bunch trains.

Extensive background calculations [4] indicate that the maximum total hit rate in the innermost layer of the vertex detector will be 0.03 hits/mm^2/bunch crossing. A typical chip size is 12.5 cm $\times 2.0$ cm. For hit rate estimates we consider a chip of this typical size

on the innermost layer. Chips at larger radius and the smaller chips in the forward disk layers will experience lower rates.

3. Progress on Monolithic CMOS Pixel Detector Design

During the past two years, working in collaboration with SARNOFF [5] through an R&D contract, we developed a conceptual design for a monolithic CMOS device (chip) that achieves the ILC vertex detector requirements and SARNOFF thinks is feasible.

3.1 General Description of the Design

The current design includes chips up to 12.5 cm $\times 2.2$ cm with $10 \ \mu$m $\times 10 \mu$m pixels. Each pixel has its electronics below and within its area, on the same piece of silicon (monolithic CMOS) thinned to a thickness of 50 to 100 μm. The electronics for each pixel records hits above an adjustable threshold. The time of each hit is stored in each pixel, up to a total of four hit times per pixel, with single bunch crossing precision (thus the name "Chronopixels" for this device). Hits will be accumulated for the 2820 bunch crossings of a bunch train and the chip is read out during the 200 msec between bunch trains. Only the coordinates (x,y,t) for hit pixels are read out. With 10 micron size pixels analog information is not needed to reach a 3 to 4 micron precision; only digital readout is planned, considerably simplifying the electronics.

The highest hit rates and occupancies result from the estimated 0.03 hits/mm²/bunch crossing for the innermost layer. With 2500 mm² per chip (a total of 25×10^6 pixels/chip) and 2820 bunch crossings per train we expect 2×10^5 hits/chip/bunch train, or an occupancy of the order of one percent.

This appears much too high to allow efficient pattern recognition. The crucial element of our design is the availability of the time information (i.e., bunch crossing number) with each hit. An event of interest at a known time in a subsystem, such as the tracker or calorimeter, are associated with vertex detector hits in time, and the occupancy is $< 10^{-5}$ per pixel (SLD worked well with a vertex detector occupancy of 10^{-3} per pixel).

3.2 Detailed Design

SARNOFF has designed the electronics under each pixel of the Chronopixel array, shown schematicly in Figure 2. The functionality of this design has been verified by an hspice simulation.

The analog components of the circuit (the boxes labeled Detector and Comparator on Figure 2) are estimated to consume most of the power, ~ 15 milliwatts/mm². The remaining digital components are estimated to be around 0.05 milliwatts/mm². The analog components are only needed during the time when hits are accumulated during the bunch train, ~ 1 msec. The average power can thus be reduced by a factor of ~ 100 by turning off the analog parts during the 200 msec digital readout. This reduces the average power consumption to the vicinity of 0.5 watts per chip or to the order of 100 watts for the vertex detector, which seems acceptable.
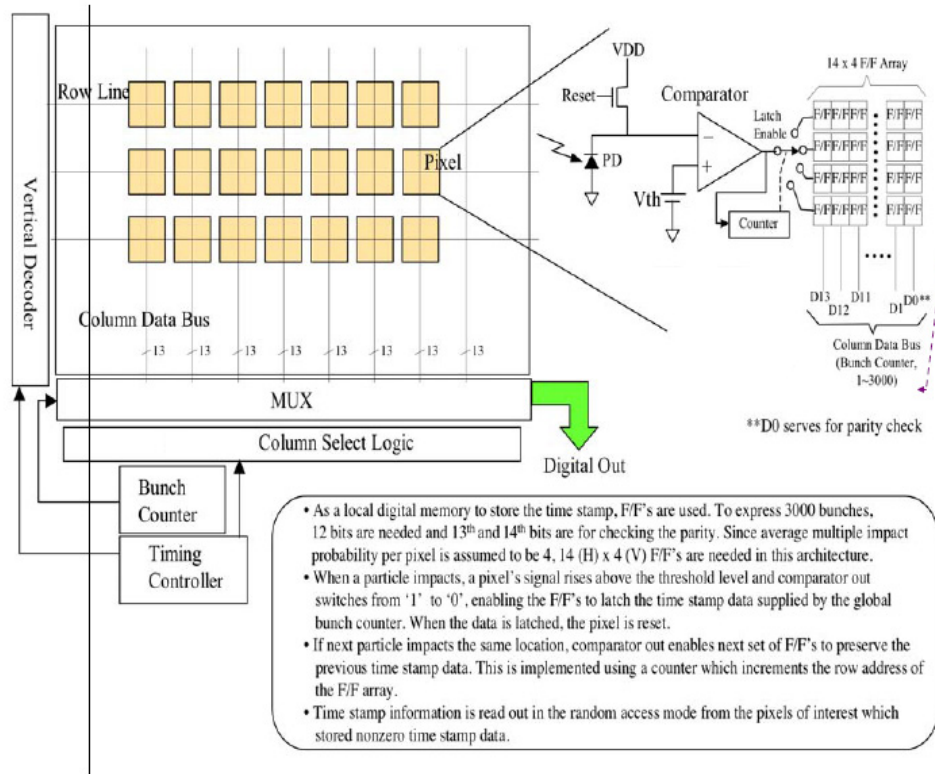
Figure 2. Chronopixel Array Architecture

3.3 Readout Scheme

Each chip will consist of 2000 columns with 12500 pixels each. Each chip will be divided into 40 readout regions of 50 columns each. At the end of the bunch train, when the electromagnetic interference due to the beam has died off, the 40 regions will be read out in parallel at 25 MHz into a FIFO buffer located at the end of each chip. The contents of the FIFO buffer will be read out at 1 GHz. We thus expect to read out the full chip (2×10^5 hits, with 38 bits per hit) in about 8 msec. This leaves a safety margin of 25 with the 200 msec gap between trains.

3.4 Other Issues

Charge Spreading. In order to be able to use digital readout the charge spreading has to be kept well below the pixel size. This can be accomplished by fully depleting the charge sensitive epitaxial layer.

   Charge Statistics and Read Noise. A Monte Carlo calculation indicates that a 1 GEV pion at normal incidence has a most probable yield of 800 electrons for a 15 micron thick

charge sensitive epitaxial layer. [6] With the read noise expected to be in the vicinity of 50 electrons the signal to noise will comfortably yield high efficiency particle detection with low backgrounds.

Process Technology. At the present time, 0.25 micron process technology is common with 0.18 micron or even 0.09 micron technology becoming possible. It does not appear possible to fit the required electronics (see Figure 2) into 10 micron × 10 micron pixels with the 0.25 micron technology; SARNOFF estimates that 0.045 micron technology will be required. The industry estimate is that 0.045 micron technology will be available by 2009, when ILC vertex detector fabrication might start. The detailed features of this technology, such as maximum voltages tolerated, etc., will be important in the realization of this project.

4. Future Plans

We plan to complete the design of those devices with SARNOFF using 0.18 micron technology this coming year with 20 or 30 micron pixels. We expect the first prototypes during the year after that. At that time we can start testing these prototypes and start on the final design with the 0.045 micron technology.

ACKNOWLEDGMENTS

References

[1] K. Abe, et al., Design and Performance of the SLD Vertex Detector, a 307 Mpixel Tracking System, Nucl. Instrum. Meth. A400, 287 (1997)

[2] C. S. J. Damerell, LCWS 2004, Paris, April, 2004, http://hepww.rl.ac.uk/lcfi/public/lcws-damerell.ppt; Y. Sugimoto, 7th ACFA Linear Collider Workshop, Taipei, Nov. 10, 2004, http://hep1.phys.ntu.edu.tw/ACFA7/slides/B-4 Sugimoto.ppt

[3] J. Brau, et al., 2005 ALCPG and ILC Workshop, Snowmass, Colorado.

[4] Takashi Maruyama, Backgrounds, 2005 ALCPG and ILC Workshop, ALCPG 0909.

[5] Sarnoff Corporation, Princeton, NJ 08540-6449.

[6] Su Dong, Private Communication.