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Monolithic CMOS Pixel Detectors for ILC Vertex Detection

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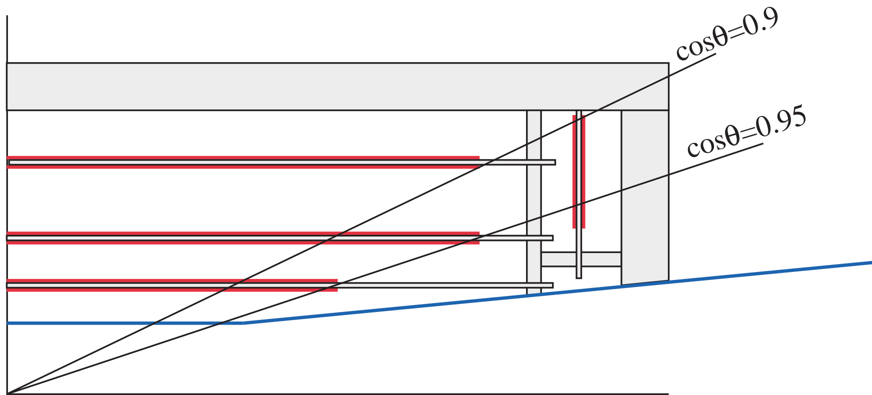
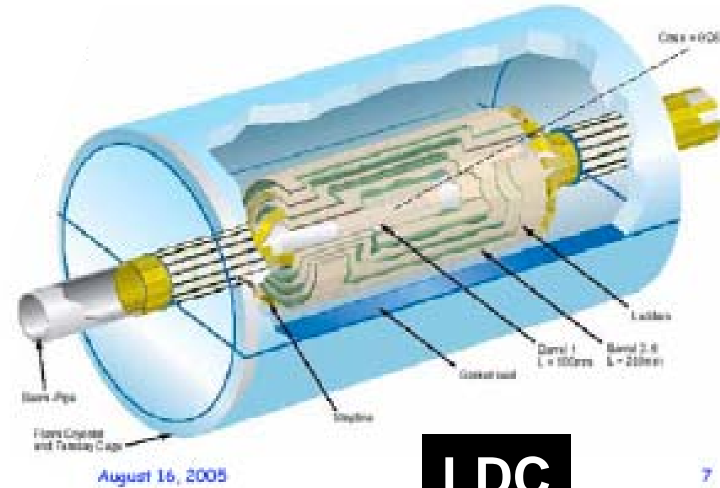
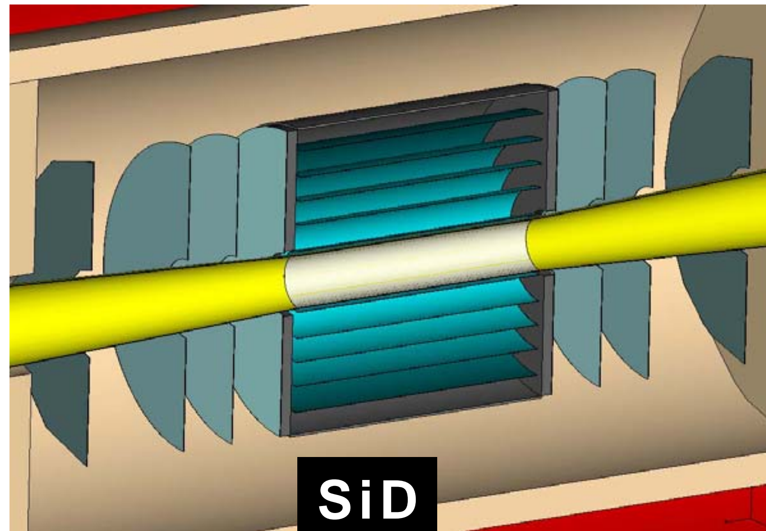
ILC Vertex Detectors

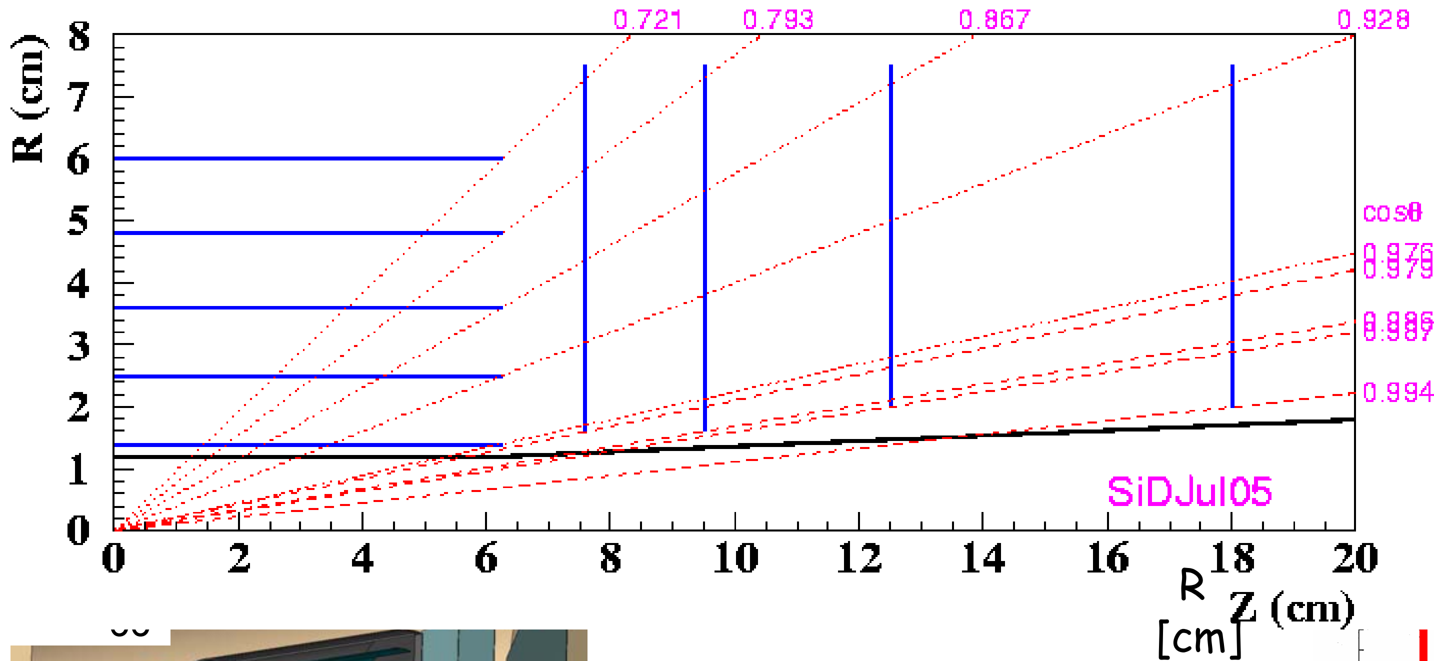


GLD

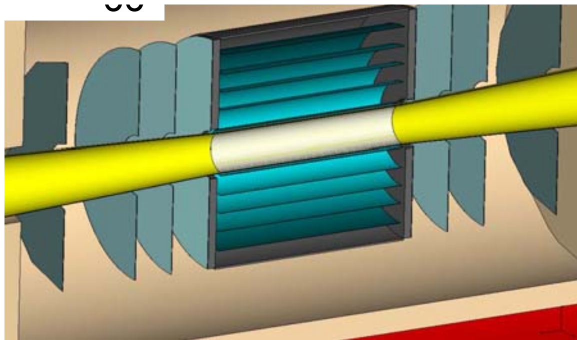




SiD Vertex Layout

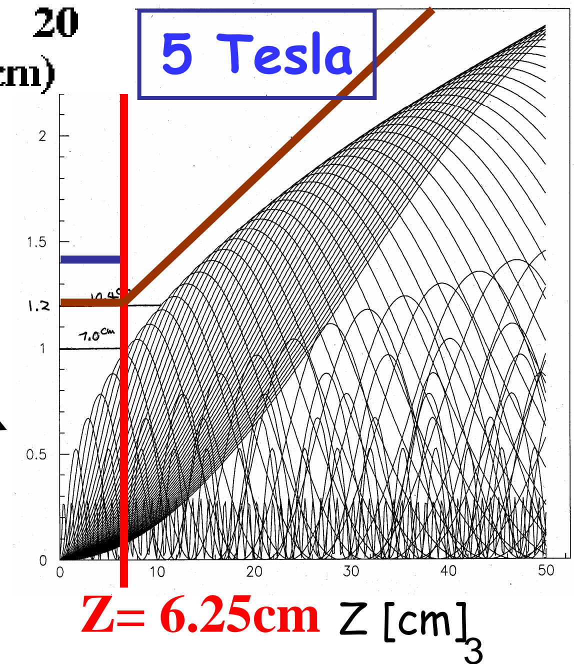


5 barrel layers
4 end disks



Design drivers:

Smallest radius possible
Clear pair background



Role:

Seed tracks & vertexing
Improve forward region

SiD Vertex Detector

- BARREL
  - 100 sensors
  - 1750 cm^2

Table I: CMOS Detector Barrel Configuration

Layer	Radius (cm)	Total Length (cm)	No. of Chips	Chip Size (cm^2)
1	1.4	12.5	12	12.5×1.2
2	2.5	12.5	24	12.5×1.2
3	3.6	12.5	20	12.5×2.2
4	4.8	12.5	20	12.5×2.2
5	6.0	12.5	24	12.5×2.2

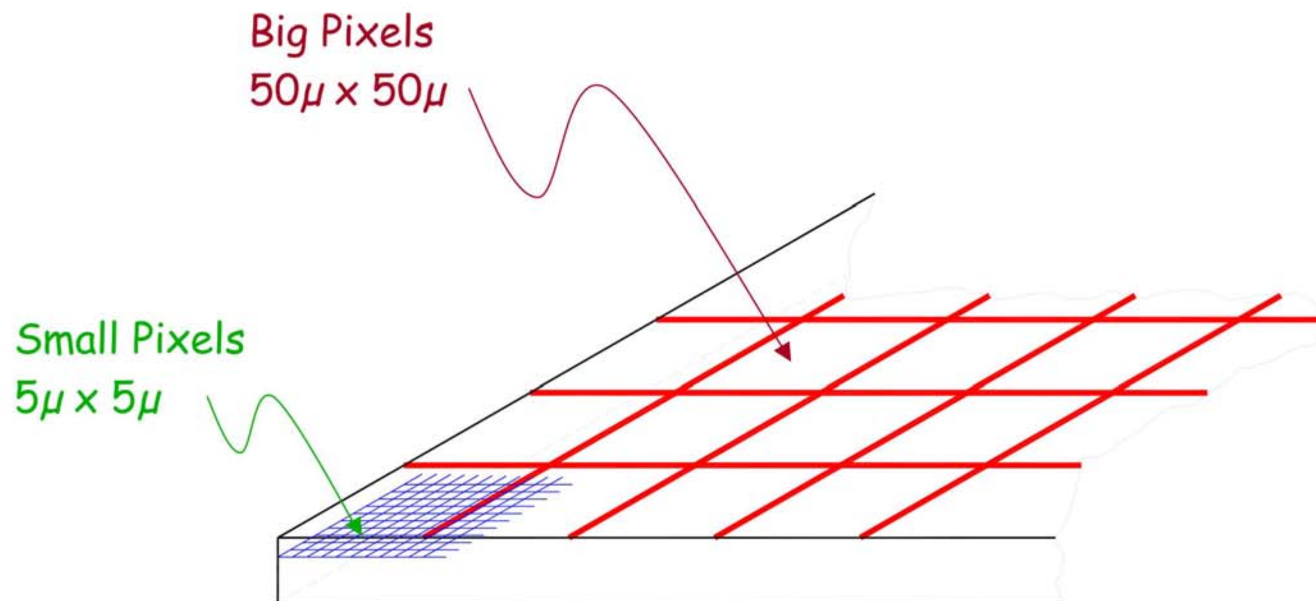
- FORWARD
  - 288 sensors
  - 2100 cm^2

Table II: CMOS Detector Forward Disk Configuration

Annulus	Inner Radius (cm)	Z (cm)	No. of Chips	Chip Size (cm^2)
1	1.6	7.6	24	1.5×0.9
	3.1	7.6	24	4.4×2.2
2	1.6	9.5	24	1.5×0.9
	3.1	9.5	24	4.4×2.2
3	2.0	12.5	24	1.1×0.9
	3.1	125	24	4.4×2.2
4	2.0	18.0	24	1.1×0.9
	3.1	18.0	24	4.4×2.2

ORIGINAL IDEA –Hierarchical array (Macro/Micro) w/SARNOFF

Monolithic CMOS Pixel Detectors



Two active particle sensitive layers:

Big Pixels – High Speed Array – Hit trigger, time of hit
Small Pixels – High Resolution Array – Precise x,y position, intensity

Summary

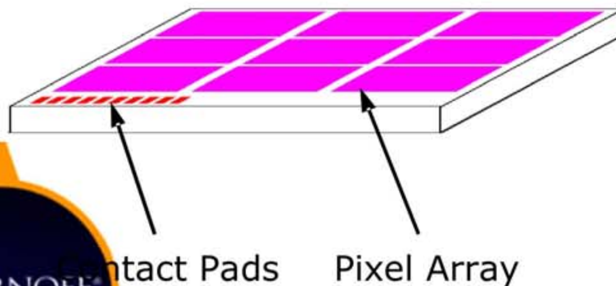
- Investigation of Hierarchical Approach
  - Macro/Micro Hybrid (50 um $\oplus$ ~5 um)

  $\Rightarrow$ Macro only, reduced to 10-15 um pixel
- Completed Macropixel design
  - 645 transistors
  - Spice simulation verified design
  - TSMC 0.18 um -> 40-50 um pixel
- Next phase under consideration
  - Complete design of Macro pixel
  - Deliverable –tape out for foundry (this year)
- Future
  - Fab 50 um Macro pixel design
  - Then, 10-15 um pixel (Macro pixel)

Array Designs

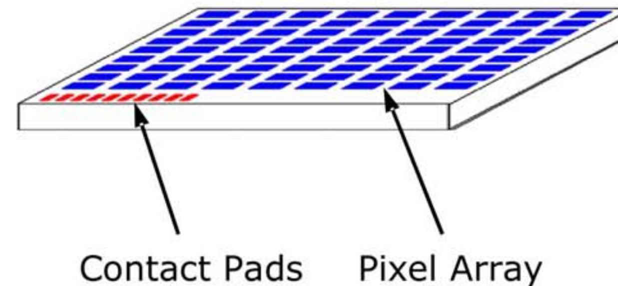
High-speed arrays

- Designed for quick response.
  - Threshold detection only.
  - Large pixels (~50 x 50 μm).
- Transmits X,Y location and time stamp of impact.



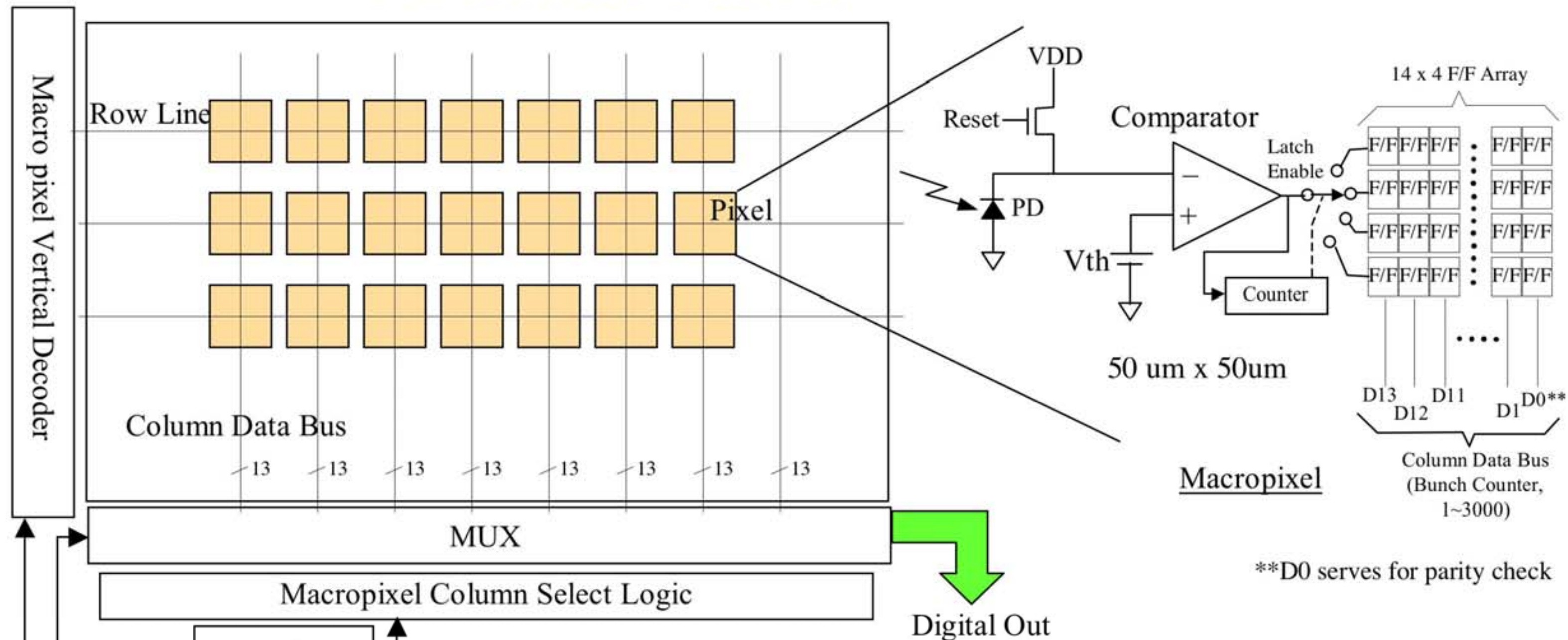
High-resolution arrays

- Designed for resolution and querying.
  - Smaller pixel size (~5 x 5 μm).
  - Random access addressability.
  - Records intensity.
- Provides intensity information only for pixel region queried.



YOUR INNOVATION PARTNER

Macropixel Array Architecture



- As a local digital memory to store the time stamp, F/F's are used. To express 3000 bunches, 12 bits are needed and 13th and 14th bits are for checking the parity. Since average multiple impact probability per pixel is assumed to be 4, 14 (H) x 4 (V) F/F's are needed in this architecture.
- When a particle impacts, a pixel's signal rises above the threshold level and comparator out switches from '1' to '0', enabling the F/F's to latch the time stamp data supplied by the global bunch counter. When the data is latched, the pixel is reset.
- If next particle impacts the same location, comparator out enables next set of F/F's to preserve the previous time stamp data. This is implemented using a counter which increments the row address of the F/F array.
- Time stamp information is read out in the random access mode from the pixels of interest which stored nonzero time stamp data.

Background Hits Dominate Vertex Detector

- Events of interest are relatively rare –
  - less than 1 Hertz.
  - hit rate in Vertex Detector dominated by background.
- Detailed calculations yield an expected background estimate of

0.03 hits/mm^2/Bunch Crossing

- However, with considerable uncertainty on this level of background.
  - Difficult calculation.
  - Background will depend on final choice of collider design details.

The Macropixel Array is Critical

- Big Pixel size (initially 50 um x 50 um) limits the tolerance to higher backgrounds.
- Therefore important to strive to reduce Big Pixel size.
  - Reducing the Big Pixel size to 10 um x 10 um
    (or even 15 um x 15 um)
    makes detector much more tolerant to backgrounds.
  - Macropixel Array (Big Pixel size) of 10-15 um might not need complement of micropixels
    - simplified design of single layer of "Macropixels"
    - with time information
    - Might not need analog information.

What Limits the Macropixel Size

- **Compress Big Pixel size, retaining storage of hit time information for 4 hits/pixel/bunch-xing**
- **Area needed with present technology (0.25 um?)**
  - Comparator/counter/latch, etc., circuit
  - Storage of up to 4 hits, i.e., 14 bits x 4 deep
- **Process Technology - how does pixel size scale as process technology goes 0.25 um, 0.13 um, etc**?
  - What do you need to go to 10 um x 10 um pixels?
  - Can you estimate the progress of this technology?
  - What's available today?
    - Much more interesting - what will be available - 5 years from now when we need to fabricate the actual devices?;
- **How much does it help to reduce max number of time stamps stored to 2 or 3?**

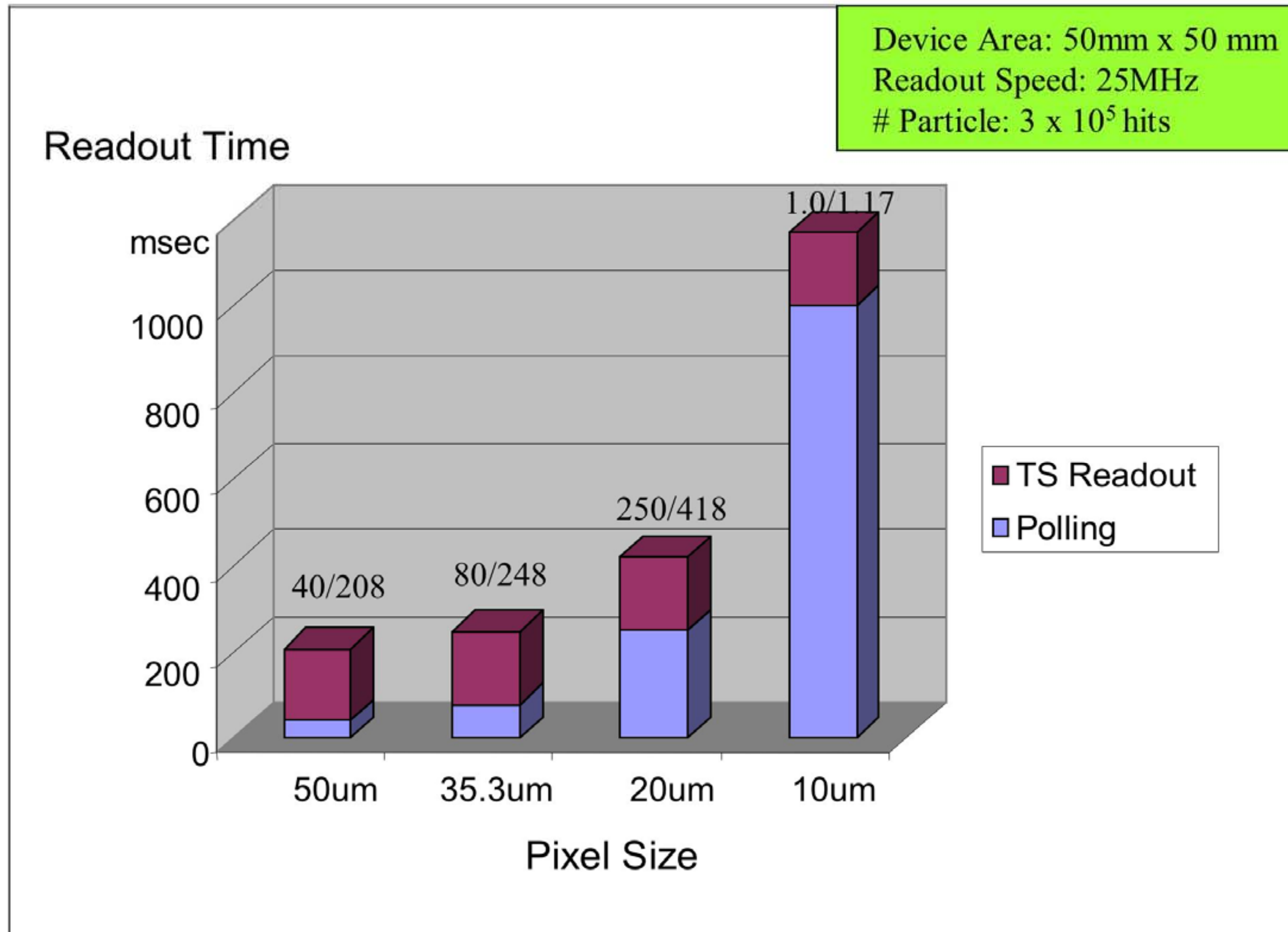
Readout Procedure and Speed

- **First, some numbers:**
  - **Consider chips 22 mm x 125 mm = 2750 mm^2 –**
  - **Total no. of 10 um x 10 um pixels = 27.5 x $1O^6$ pixels/chip –**
  - **Total hits .03 x 2820 x 2750 = 2 x $l0^5$ hits/chip/bunch train**
- **How long does it take to interrogate a pixel to see if it has a hit (presumably look of a single bit flag?)**
- **How long does it take to read out one hit pixel**
  - **X info (up to 2200) - 12 bits + parity = 14 bits**
  - **Y info (up to 12500) - 14 bits + parity = 16 bits**
  - **Time (up to 3000) - 12 bits + parity = 14 bits**

    44 bits total
- **2 x 10^5 hits/chip x 44 bits/hit / 50 MHertz = 176 msec**
- **Might divide each chip into parallel readout streams (10-20) to accommodate higher background rates?**

SARNOFF Response to Question

Estimation of Overall Readout Time vs. Pixel Size

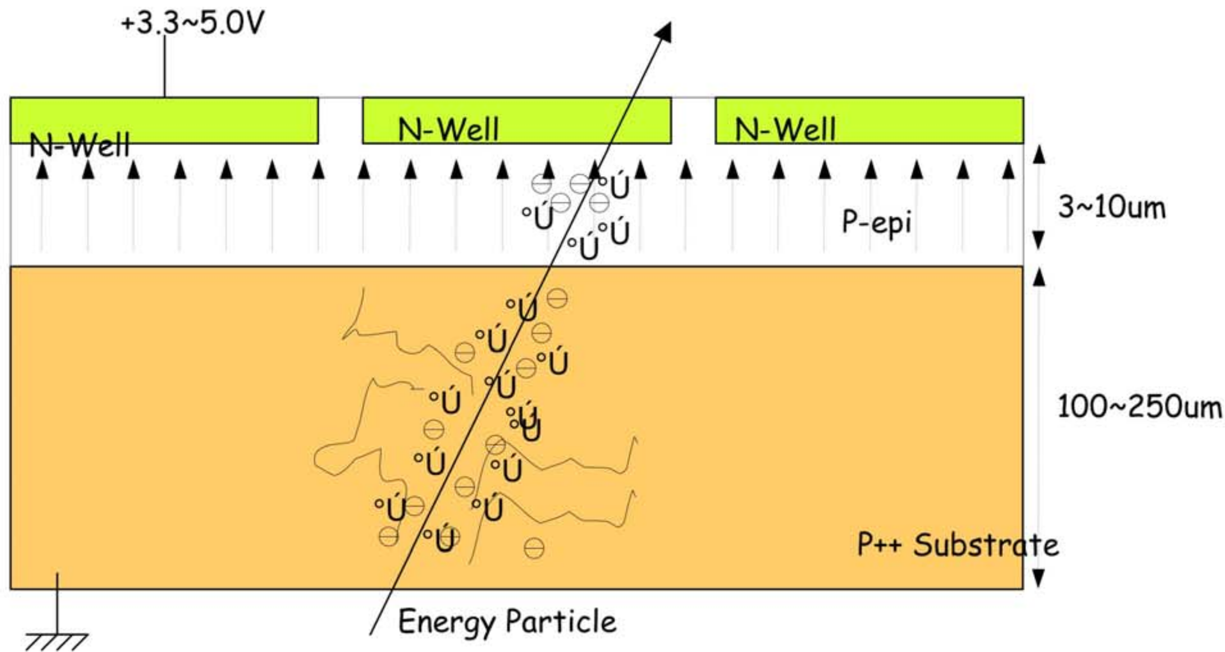


Charge Spreading

- Important to minimize charge spreading
  - pixel size sets scale that would reduce need for analog information.
- How small can we keep the charge spreading?
  - Thickness of expitaxial layer - 10 to 15 um
  - Possible approach - full depletion of epitaxial layer
    - requires high resistivity? - few kohm-cm? or less?
  - Depletion voltage, field in epilayer?

SARNOFF Response to Question

CMOS Pixel and Vertical Cross Section



- Entire P-epi region is assumed to be depleted and p++ substrate region is not depleted.
- Electron is the minority carrier in p++ substrate and p-epi.
- Electrons generated in the p++ substrate will diffuse around but can not travel far because they recombine quickly with holes that are abundant in the p++ sub.
- Electrons generated in the epi-region are forced move toward N-well diode region by the electric field and do not have the chances of recombination.
- In conclusion, spread is minimum even if the CMOS wafer is not thinned. Epi-thickness and electric field are the factors to determine the lateral spread function.

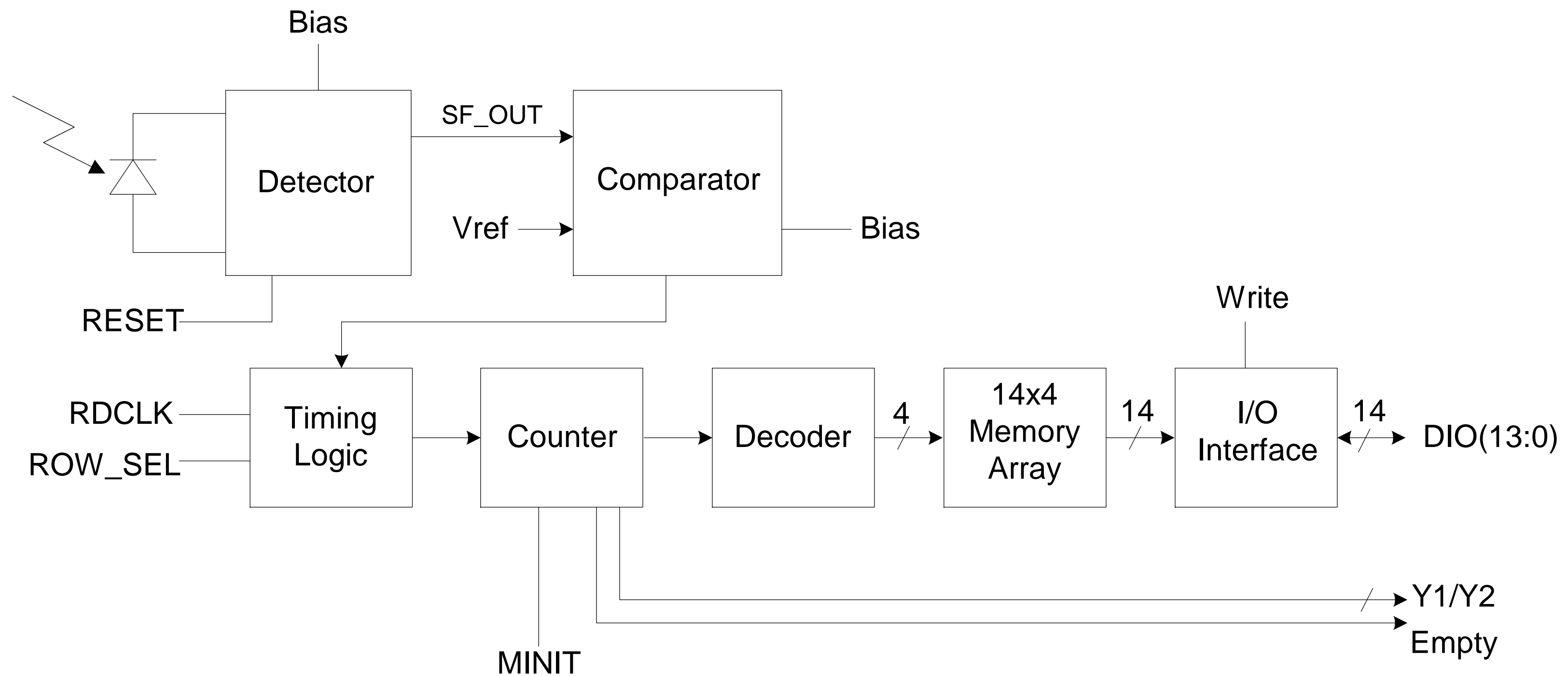
Read Noise

- Minimum ionizing particle leaves ~ 88e$^-$ /micron in expitaxial layer
  - **10 um** thick epi x 88e-/um = ***880 electrons***
- GOAL - signal to noise of 10 to 20
  - Can we keep read noise below 50 e- or so**?**
  - This consideration determines thickness of the exitaxial layer.

Power Consumption

- Keep power to ~100 millwatts/chip (goal)
  ~4 mW/cm^2
- Trade-off noise with power
- Make design choices which optimize noise/power tradeoffs

Macropixel Block Diagram



Power Dissipation Analysis

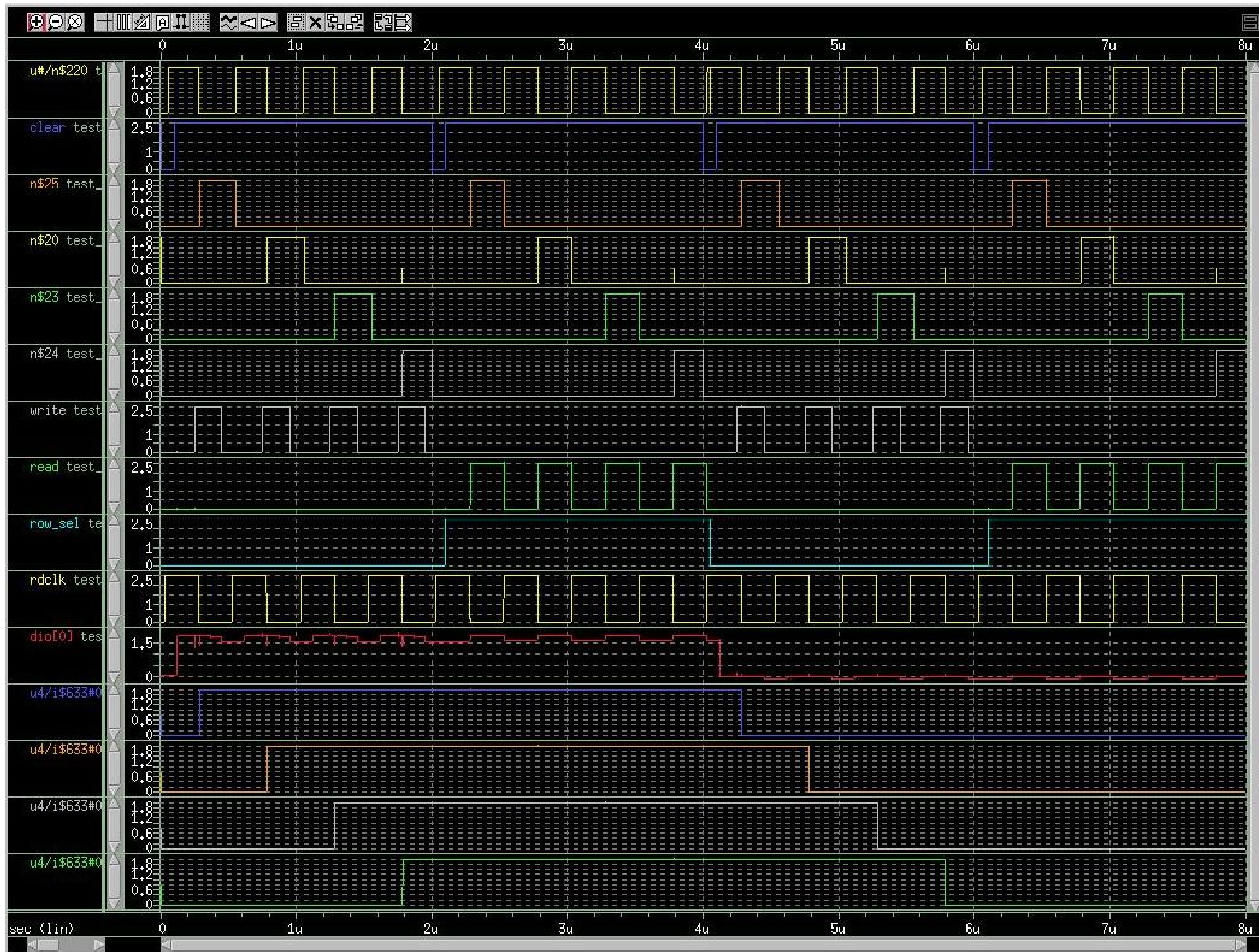
	Component	Optimized Power Dissipation	Before Optimization
Analog	Detector	9.9uW	11.7uW
	Comparator	27.0uW	35.1uW
	Sub_total	36.9uW	46.8uW
Digital	Timing Logic	0.05uW	
	Counter/Decoder	0.07uW	
	Mem. Array	~ 0uW	
	IO Interface	0.01uW	
	Sub_total	0.13uW	
	Total	37.03uW	

- Additional 67- to 100-fold reduction expected by power cycling analog components (0.37 – 0.55 uW)

Other Considerations

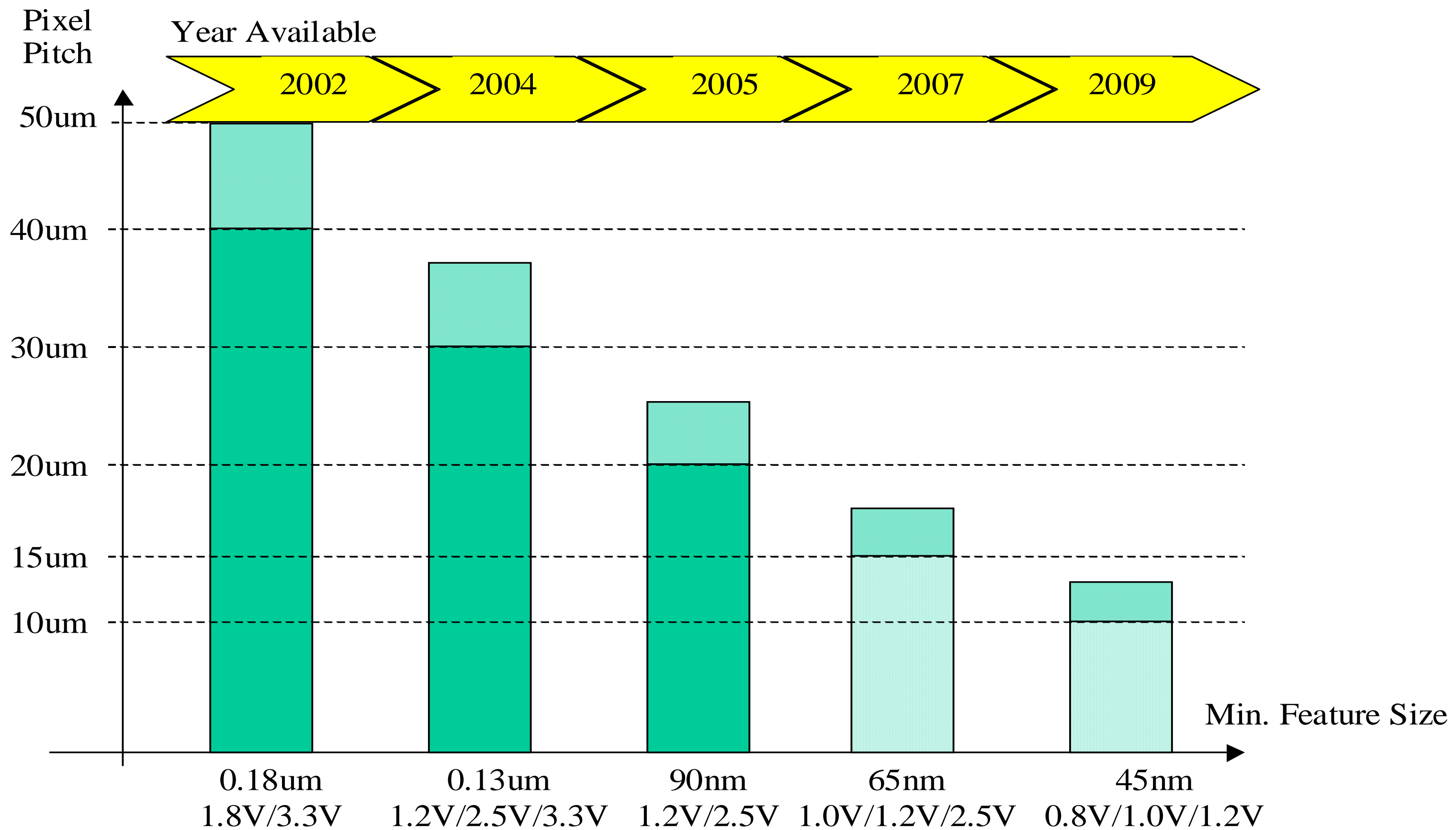
- Dark Current
  - Keep it small
  - Sarnoff – will reset array on each bunch
    - Should not be a problem
- Operating Temperature
  - Sarnoff expects modest cooling ($\lesssim 0°$C adequate)
- Device Thickness
  - Thinning below 50 um looks feasible
- B Field – Lorentz angle

Spice Model Verification of Design



SARNOFF Response to Question on Future

Technology Roadmap: Macropixel size estimation vs. Mixed-signal Process Technologies



CONCLUSION

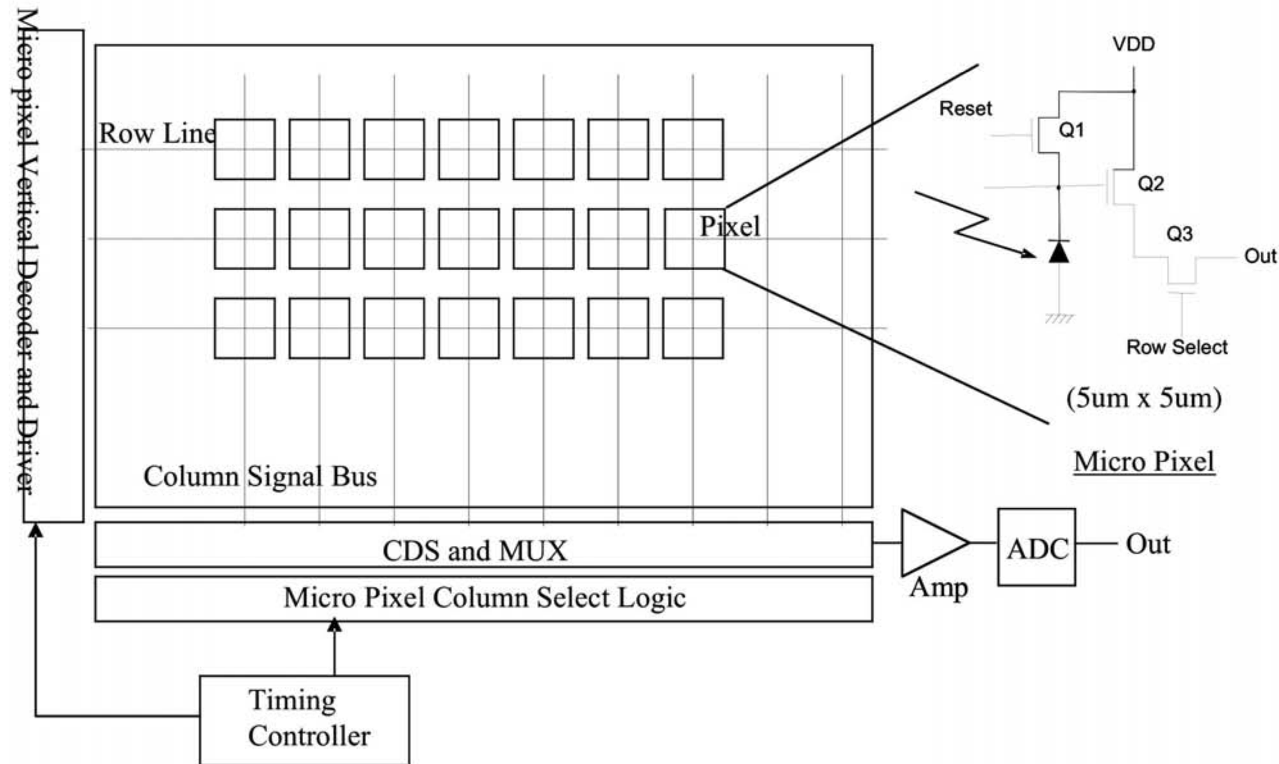
- Completed macropixel design
  - 645 transistors
  - Spice simulation verifies design
  - TSMC 0.18 um -> 40-50 um pixel
- Next phase under consideration
  - Complete design of macro pixel
  - Deliverable –tape out for foundry
- Future
  - Fab 50 um pixel chip
  - Then, 10-15 um pixel

EXTRAS

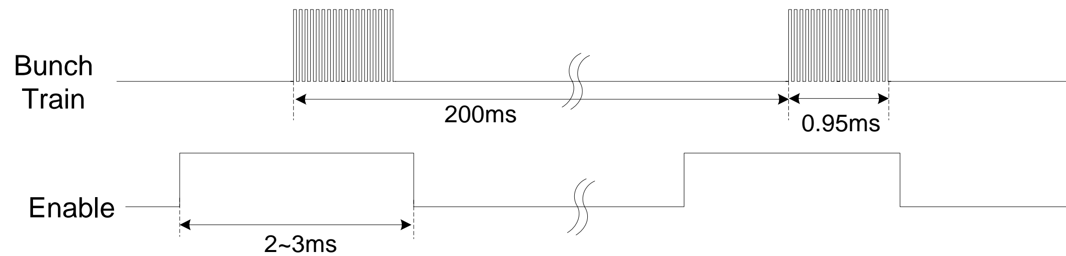
Possible Plan of Action

1. Start with estimating the parameters (Big Pixel size, etc.) that we can expect to build in ~ 5 years
2. Work toward an ultimate design with:
   a) Single layer of Macro Pixel Array
   b) Approach 10 μ x 10 μ pixels
   c) Detect hits above some threshold
   d) Store up to 3 or 4 time stamps/pixel
   e) No analog information
   f) Approach other parameters discussed
3. Detailed Design of Macropixel Array
4. Build prototype with whatever pixel size possible at that time for testing and proof of principle
5. Plan to build ultimate devices ~ 5 years from now

Micro Pixel Array Architecture

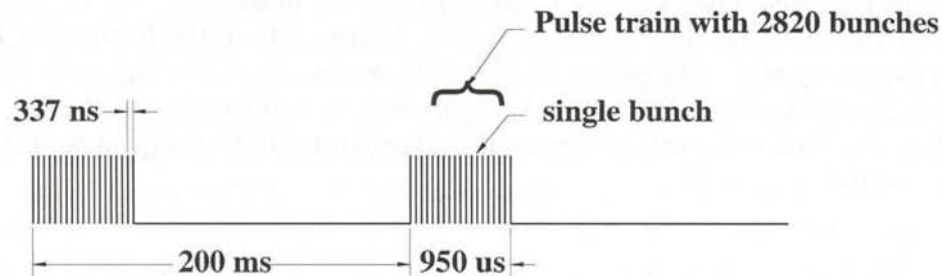


Power Reduction Method



- Activate the Detector and the Comparator during the Bunch Train and deactivate rest of the time
- Power Reduction Ratio = 1/67 to 1/100 (0.552 μW to 0.37 μW)

Time Structure for the TESLA Design



Background Calculation:

At 1.5 cm from Interaction Point with 3 Tesla field expect

0.03 hits /mm^2/bunch crossing

Will use this number for the entire detector