Pixel Detector Work at Oklahoma and LC Proposals

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Possible Technological Options

- **CCD**: Thickness of the sensitive region ~ 20 µm
  Wafer thickness can be thinned down to ~ 20µm
  Relatively sensitive to radiation damage

- **CMOS pixel sensor**: Sensor diode and read-out amplifier
  Signals from pixels are read out by X-Y addressing
  Thickness of the sensitive region ~ 20µm
  Radiation immunity is better than that of CCDs

- **Hybrid pixel sensor**: Sensor diode wafer and readout wafer connected
  by bump bonding technique
  Thicker than CCDs or CMOS sensors
  Radiation hardness is excellent
LC Software Interest (DOE)

- Monte Carlo studies of Silicon Tracker and/or CCD Detector
  - Optimize design, including number of layers, forward region (pixels?)
  - Test and develop pattern recognition. How many layers are necessary?
- Past Experience (Mike Strauss)
  - Developed clustering algorithms, and track finding for SLD VXD2, and optimization of VXD3 design.
  - Developed Monte Carlo simulation of VXD2 and VXD3 including charge deposition and integration.
  - Developed pattern recognition and track finding for TPC at PEP.
LC Hardware Interest (NSF)

- CCD Research and Development
  - Test properties of CCDs
    > Help answer questions about use of CCDs in LC environment.
  - Develop new CCD support technology, particularly electronic connections and components
  - Thinning and radiation tests, establish relationships with vendors
  - Readout design, DAQ (UCLC proposal)

- Past Experience
  - Tested microstrip detectors now installed in DO, CLEO III
  - Developed flex connectors for CLEO III
  - Developing and testing flex circuits for ATLAS Pixel detector
  - Contributed to ATLAS pixel readout design
<table>
<thead>
<tr>
<th>Name</th>
<th>EE Masters Thesis Title</th>
<th>Year</th>
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<tbody>
<tr>
<td>Gorthy, A.</td>
<td>Standard Cell Characterization of the CMOS Deep-Submicron Library</td>
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<td>Sriram, S.</td>
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<td>Krishnama, S.</td>
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<td>VLSI Design for the Portcard in Silicon Strip Detector Experiments</td>
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NSF Proposal

- A UCLC proposal was submitted: “Development and design of an LC ASIC for CCD readout and data reduction”
- Three year project
- Collaboration between OU, Boston U. (Ulrich Heintz), and Fermilab (William Wester)
- Previous experience on ATLAS pixel detector which uses IBM deep-submicron process
- Fermilab may contribute designer starting soon (Jan. 2003?)
Readout speed challenge

- **Requirement for NLC/JLC** ~8 msec readout time
- **Requirement for TESLA** ~50 μsec (due to large number of bunches in a pulse train)
- VXD3 readout time is 200 msec with 5 MHz clock speed and 4 output nodes/CCD. Clock speed 10 MHz was tested – no problems. 50 MHz clock speed was tested by UK group. It works. Remaining factor of 2.5 in reduction of readout time can be achieved by increasing number of outputs. 12 - 16 outputs/CCD will do the trick for NLC/JLC.
- Task for the TESLA is more challenging, but also feasible. UK group has reported arrival of first prototype CCD with *column parallel readout*. Essentially this is equivalent to increasing number of outputs per CCD to hundreds or even thousands. There are electronics challenges on this way, mainly related to power dissipation on CCD. However, taking into account duty factor of about 200 for TESLA, pulsed power may solve such problems.
Column Parallel CCD (from talk by Konstantin Stefanov)

- Serial register is omitted
- Maximum possible speed from a CCD (tens of Gpix/s)
- Image section (high capacitance) is clocked at high frequency
- Each column has its own amplifier and ADC – requires readout chip
Readout speed challenge – more

Tread = Nrows * (Ti + Ncol * Tr)
For VXD3 Ti=20 μsec Tr=200 nsec
Nrows = 2000, Ncol=400, Npix=8x10^5
(per node, per CCD Npix=3.2x10^6 )
For TESLA assume Npix same, Tr=0
Because of absence of R register,
Nrows = Npix/Nnodes ~ 1000.
To get Tread=50 μsec Ti should be 50
nsec, meaning 1 clock frequency 20 MHz
But capacitance of 1 clock bus is 40 nF
instead of < 100 pF for R clock bus.
Its impedance for 20MHz is 0.2 Ω , which
leads to 1 clock current ~50 A/CCD (with
10 V clocks).
Personnel

- **OUHEP**
  - Electronics Engineer (Base program)
  - EE Master’s student (ASIC design)
  - Test facilities

- **BU**
  - ASIC designer
  - Graduate student
  - Test facilities

- **Fermilab (Base program)**
  - ASIC design group
  - Test facilities
  - Silicon lab
OUHEP Equipment

- Clean room
  - Probe station
  - Voltage/Current sources
  - C, R, V, I meters, scanner
  - VXI system
- New equipment (from NSF MRI grant)
  - Automatic wire bonder
  - Optical comparator
  - Plasma cleaner
  - Environmental chamber
  - Logic Analyzer
Clean Room
Test Instruments controlled by Labview Program
Westbond 2400B Au Ball & Wedge, Al Wedge Bonder
Conclusions

- UCLC proposal has been submitted
- Work could begin now
- We would welcome discussions with others interested in vertex detector readout
  - Oregon/Yale group
  - LCFI group
  - etc.