6 Field Effect Transistors

Field effect transistors (FETs) come in a myriad of different configurations and types, but they generally belong to two broad classes: depletion-mode devices like JFETs or enhancement-mode devices like MOSFETs. In either case, the functional difference of a FET from a bipolar junction transistor is the extremely high input impedance of the device from the control input. The tradeoff for this high input impedance is usually a much lower equivalent gain than a BJT, which makes FETs particularly suited for input stages to amplifiers and other instrumentation. The other common use of FETs is as a voltage-controled analog switch, and in fact the vast majority of digital electronics devices are constructed from large numbers of complimentary MOSFET (CMOS) switches.

6.1 FET connections

Figure 30 shows the basic connection definitions for a JFET transistor. Confusingly, the naming convention for FETs is different from BJT, with a Drain, Gate, and Source taking the place of a Collector, Base, and Emitter. FETs come in both n-type and p-type variants just as BJTs do, and for simplicity will restrict ourselves to talking about n-type FETs.

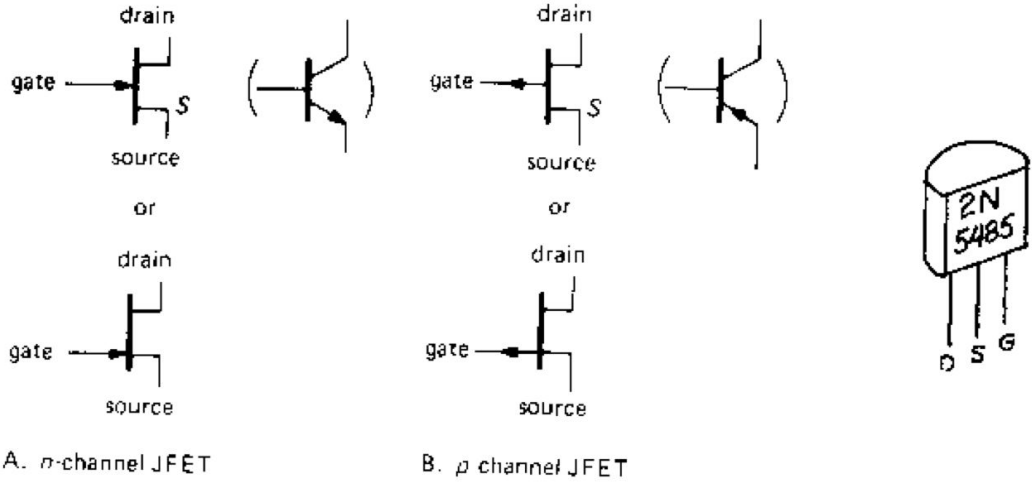

Figure 30: JFET transistor connections.

6.2 FET geometry

Figure 31 shows the geometry of a JFET and MOSFET transistor. In the JFET, the gate forms a PN (diode) junction with the N-doped silicon which forms the bulk of the device. This structure, also known as a depletion-mode device, acts as a conductor from source to drain as long as the gate voltage is near the source voltage. When the gate is biased with a negative voltage, this depletes the negative charge carriers (electrons) in the region under the gate, and the conductance from drain to source is reduced. With enough negative voltage,

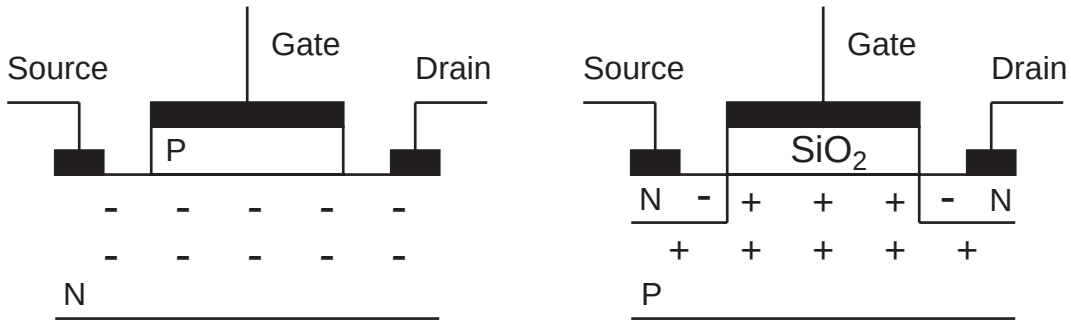

Figure 31: JFET (left) and MOSFET (right) transistor geometry.

usually called V_P or the pinch-off voltage, the JFET is fully depleted and no charge will flow. The action of a JFET, then, is to normally conduct unless a negative voltage is applied to turn it off.

The MOSFET works in the opposite manner. Note that in a MOSFET, the gate is electrically insulated from the silicon underneath by a layer of something like silicon dioxide, making it nearly impossible for any current (at least DC current) to flow from the gate to source or drain. There is no natural conduction channel between the embedded N-type regions because they are blocked by the P-type region. A positive bias on the gate will push the positive carriers out of a region in the P-type silicon between the drain and source, opening up a conduction region. This enhancement of the conduction means the MOSFET is normally non-conducting unless a positive voltage is applied to turn it on.

6.3 FET operating conditions

The depletion-mode and enhancement-mode devices differ in their operating details, but in general the operation of both can be understood in terms of the gate voltage above some threshold voltage $V_{GS} - V_T$. For a JFET, this threshold will be a few volts negative, while for a MOSFET, this threshold will be around ground. In both cases, a voltage difference of 3-5 volts will be necessary to fully turn on the device.

FETs are pure transconductance devices, meaning that the current flowing from drain to source I_D is function of the gate-source voltage difference V_{GS}. We will see it can also be a function of the drain-source voltage difference V_{DS} when V_{DS} becomes small. As long as V_{DS} is larger than a few volts, however, the FET acts as a pure current source with I_D being controlled by V_{GS}. For small signals, we define the relation $i_d = g_m v_{gs}$, where g_m is called the transconductance of the device.

When $V_{DS} > (V_{GS} - V_T)$, the FET is said to be operating in the "saturated region", which confusingly is just the opposite of the meaning of a saturated BJT (where V_{CE} is small). For the saturation region, we find the drain current is given by

$$I_D = \kappa(V_{GS} - V_T)^2$$

independent of V_{DS} and quadratic in $V_{GS} - V_T$. Again, V_T depends upon device type and varies quite a bit from device to device, but for a JFET, this will be about around -3 volts, while for a MOSFET it will be near zero.

When $V_{DS} < (V_{GS} - V_T)$, the FET is said to be in the "linear region", and we find

$$I_D = 2\kappa[(V_{GS} - V_T)V_{DS} - \frac{1}{2}V_{DS}^2].$$

In the small V_{DS} limit, the second term can be neglected, and the drain current is linear in $V_{GS} - V_T$, as well as in V_{DS}. This linear relation between I_D and V_{DS} means that the FET looks like a resistor from drain to source, with a resistance of $1/R = 2\kappa(V_{GS} - V_T)$, controlled by V_{GS}.

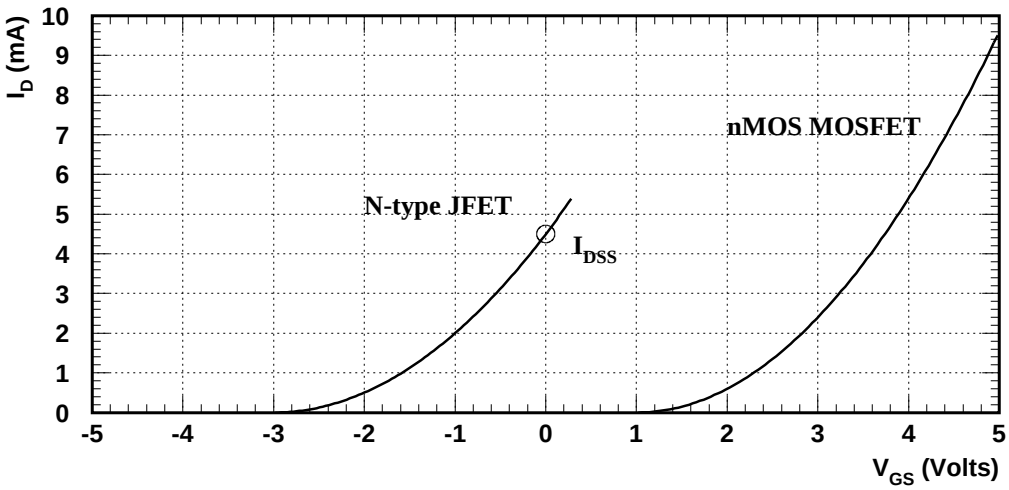

Figure 32: Drain current vs. gate-source voltage for saturated FETs.

Figure 32 shows $\log I_D$ vs. V_{GS} for a JFET and MOSFET operating in this saturated region. Note that a JFET gate should not be forward biased to its source, and as a result the max current delivered by a JFET will be at $V_{GS} = 0$. This current, when the gate is shorted to the source, is called I_{DSS} and is typically 5-10 mA. If $V_{GS} - V_T$ was larger than V_{DS}, the device would enter the linear region, and the current would then only grow linearly with V_{GS} rather than as V_{GS}^2.

Figure 33 shows the I-V curve (I_D vs. V_{DS}) for a MOSFET (although a JFET would look quite similar) illustrating the linear and saturation regions. The curves are drawn for increasing $V_{GS} - V_T$ which gives a quadratic increase in the current in the saturation region on the right. A JFET would have a maximum current of I_{DSS} when $V_{GS} = 0$.

6.4 JFET current source

Because a JFET delivers a fixed current I_{DSS} when $V_{GS} = 0$, this makes a very handy and quick way to build a current source, as shown on the left in Figure 34. The actual current provided will vary greatly depending upon the specific value of I_{DSS} for any given JFET, but there is no easier way to get a few mA current source. The drain current for $V_{GS} = 0$ is $I_D = \kappa V_P^2$ which is the definition of I_{DSS} (drain current with gate shorted to source). From this we can extract the constant $\kappa = I_{DSS}/V_P^2$ for a JFET. Typically, a JFET will be characterized in terms of I_{DSS} and V_P, and from these two values, most of the rest of the operating characteristics can be derived.

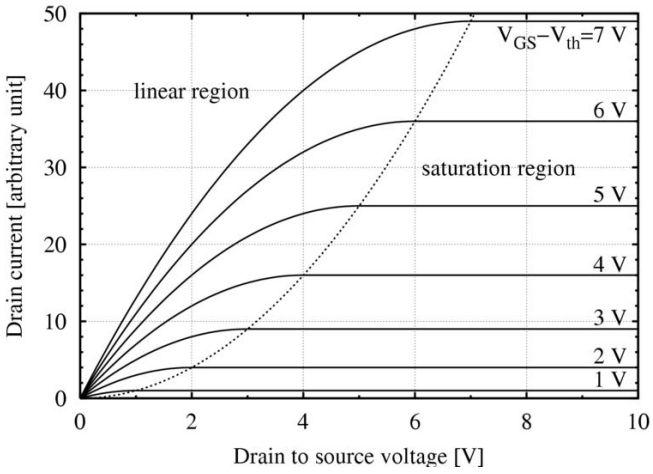

Figure 33: I-V curves for a typical MOSFET.

Using this expression for κ, we can rewrite the current provided by a JFET as

$$I_D = I_{DSS}(1 - V_{GS}/V_P)^2,$$

so by making V_{GS} more negative, we can reduce I_D. A circuit to do this is shown on the right of Figure 34. The added resistor provides $V_{GS} = -I_D R$ which will reduce $V_{GS} - V_P$ and hence I_D. If you want a specific current, you can either solve for R using these two equations, or more easily draw a quadratic function for I_D vs. V_{GS} and intersect this with a straight load-line to indicate the resistor. The slope of that line giving the desired current is $1/R$.

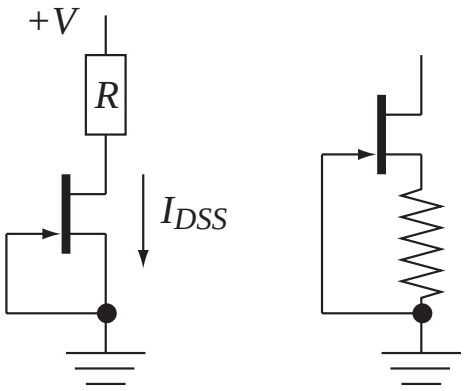

Figure 34: Simple JFET current source (left) and adjustable current source (right).

6.5 Transconductance

A FET is a pure transcounductance device, with no current flowing from gate to source, and the drain current determined by the relation $g_m = \Delta I_{out}/\Delta V_{in} = i_d/v_{gs}$. The parameter g_m

is the transconductance of the device, and has units of 1/resistance. We saw this idea already with BJTs that there was an effective internal emitter resistance of $r_e \approx 25$ ohms. One feature of FETs is that they have significantly larger internal resistance values $1/g_m \approx 200 - 2000$ ohms, meaning that they have significantly reduced "gain" compared to a BJT.

From what we have already seen, g_m is clearly dependent upon V_{GS}, but also upon V_{DS} in the linear region. Unlike the notion of β in a BJT, g_m for a FET can not be simply approximated as a constant, which makes design of FET circuits somewhat more annoying.

One confusing issue is the units of transconductance. A simple way to think of this is in units of 1/ohms, as long as you realize the conductance isn't constant. The SI unit of conductance (or transconductance) is called the siemens (1 S = 1 A/V). A 100Ω resistor would have a conductance of 1/100 = 10 millisiemens (mS). There is also an older unit of "inverse ohms" or mhos which our book sometimes uses which is the same as the siemens (1/ohm = 1 mho). We will try to stick with 1/ohm to avoid confusion.

6.6 JFET transconductance

For any device, the conductance is the slope of the I-V curve. For a JFET in the normal operating saturation region, $g_m = dI_D/dV_{GS} = 2\kappa(V_{GS} - V_P)$. Replacing κ we can rewrite this as $g_m = 2/V_P\sqrt{I_{DSS}I_D}$. Putting in typical values of a few milliamps and a few volts, we see this will have a transconducance g_m on the order of 1 mS, or $1/g_m \approx 1\text{k}\Omega$.

Note that the transconductance is linear in V_{GS} and proportional to the $\sqrt{I_D}$, reaching a maximum at I_{DSS}. Compare this to the equivalent expression for a BJT, where $1/r_e = 25\text{mV}/\text{I}_\text{C}$, linear in I_C, and with a typical magnitude of $1/25\Omega^{-1}$ or 40 mS. Clearly the ability of a JFET to amplify a signal will be much worse than a BJT.

6.7 JFET voltage amplifier

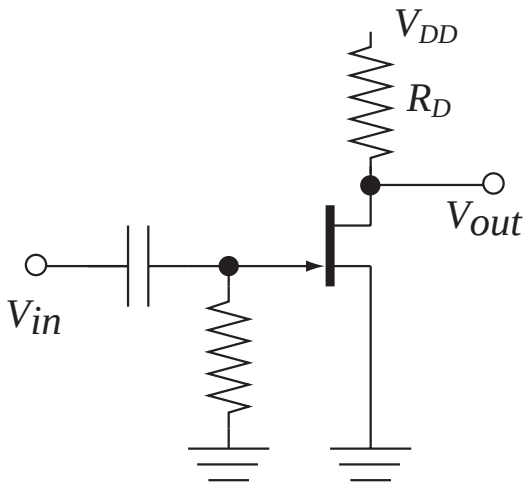

Figure 35: JFET version of a common-emitter amplifier.

We can take our typical circuit for a common-emitter amplifier and directly replace the BJT with a FET device. If we use a JFET, we can make several simplifications, as shown

in Figure 35. First, the JFET is happy to run with V_{GS} near ground, so we don't need the voltage divider to bias the gate away from ground. A single (large) resistor to allow variations in V_{in} is enough. Second, as we saw in our current source, the JFET doesn't really mind having the source grounded either. It doesn't hurt to have a resistor here, but the circuit analysis is actually simpler without it, so we will drop it for now.

So how do we analyze this circuit? First, with $V_{GS} \approx 0$, the quiescent current will be given by $I_D = I_{DSS}$. The output voltage will then be biased at $V_{\rm out} = V_{DD} - I_D R_D$. Adding a resistor to the source leg will reduce I_D and can be used to change the output bias voltage. So can changing R_D.

To find the gain, we need to look at the small-signal response. $v_{\rm out} = v_d = -i_d R_D$, while $i_d = g_m v_{\rm in}$. Putting these two relations together, we find

$$G = \frac{v_{\rm out}}{v_{\rm in}} = -g_m R_D.$$

To be more concrete, consider a JFET with $V_P = -2.5$V, $V_{DSS} = 5$ mA, and use $R_D = 1\text{k}\Omega$. Our transconductance $g_m = 2\sqrt{I_D I_{DSS}}/V_P = 4$mS. Another way to look at this is $1/g_m = 250\Omega$. The gain, then is $g_m R_D = -4$, which isn't very large. The gain is limited by the small g_m, or in analogy with the BJT case, the effectively large resistance provided by $1/g_m$. Adding a source resistor will only make this worse, as the series resistance to ground will increase, plus by reducing I_D you will also reduce g_m.

6.8 JFET follower

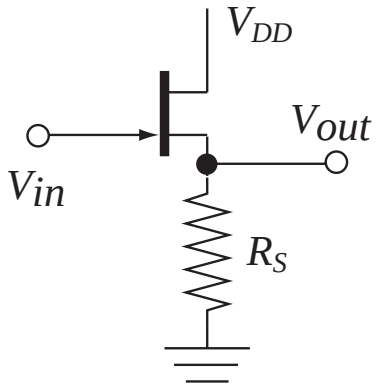

Figure 36: JFET follower.

Figure 36 shows a JFET version of a follower. This circuit has a very large input impedance, due to the absence of any current flowing in through the JFET gate. The relatively low transconductance, however, makes this circuit a little problematic.

Here, $v_s = i_d R_S$ and $i_d = g_m v_{gs} = g_m(v_g - v_s)$. Now, $v_s = v_{\rm out}$ while $v_g = v_{\rm in}$, and solving for $v_{\rm out}$ yeilds the relation

$$\frac{v_{\rm out}}{v_{\rm in}} = \frac{g_m}{1/R_S + g_m} = \frac{R_S}{R_S + 1/g_m}.$$

Not surprisingly, this looks something like a voltage divider, with the output attenuated by going through the effective impedance $1/g_m$ and the resistor R_S. With values of $1/g_m$

possible up to 1 kOhm, this resistance can't be neglected, and typically the gain will be less than one, for modestly-sized R_S. Compare this to a BJT follower, where $r_e \approx 25$ Ohms, and this resistance can be completely neglected.

The advantage of a JFET follower is the huge (nearly infinite) input impedance. A drawback is the poor output impedance, and non-unity gain. This will again be dominated by the effective resistance $1/g_m$ which could be of order 1 kOhm. One way to improve this is to attach a current source (sink) to the source leg to provide an effectively infinite resistance. This can be done using something similar to Figure **??** to provide a complete follower circuit with large input impedance and unity gain using nothing much more than two JFETs. Most modern oscilloscopes have a circuit very similar to this for their input stages.

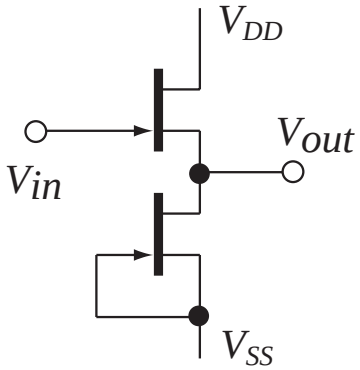

Figure 37: JFET follower with current source.