Parts List

- ICs: 7404, 7493, 74150, 74154, TIL311

Note: Each section of this lab largely builds upon the section before it. If you plan a little carefully, you can minimize the amount of rewiring you will have to do.

If you want to work with a partner this week, that is fine. Each person should fill out their own lab notebook, however. Share the work of wiring up the circuit and double-checking the results.

Always make sure you TURN OFF THE POWER when inserting or removing ICs.

2.1 Decoder

A decoder uses an input address to select one of many possible outputs. Multiplexers use a decoder to select which input line gets sent to the output. The 74154 IC is a 4-bit decoder/multiplexer. It is used here to decode a 4-bit binary number (the 4 address inputs) to select one of \(2^4 = 16\) possible outputs.

Construct the circuit shown in Figure 1 below. The 7493 is a 4-bit binary counter. We will learn more about counters later, but its basic function is simple: It counts the number of pulses input on pin 14. The 4 binary digits representing this count are output on pins 12, 9, 8, and 11, as shown. We are using these 4 bits of counter output simply to set up different addresses for the decoder.

Use a debounced switch on your prototype board to generate the counter input pulses. It is usually smart to build parts of a circuit at a time and check that they are working before adding more complexity. Start with a debounced button, the 7493, and the TIL 311. Check that the counting is proceeding correctly before adding the 74154 to the circuit. With the completed circuit, toggle through all address inputs to the 74154 and measure the state of the 16 outputs. The outputs can be measured using a scope, logic probe, DVM, or the LEDs on your prototype board. Determine and record the truth table for the 74154. Are the outputs “positive true” or “negative true”? (Note: on the 74154, pin 12 is not an output!)

2.2 Multiplexer–Demultiplexer

Now modify the circuit with the additions and changes shown in Figure 2 below. The circuit now consists of a multiplexer or MUX (74150) which sends data from 16 possible inputs to a demultiplexer or DEMUX (74154) over a single data line. (In the previous section, the data input at pin 18 of the 74154 was held at ground. Since it uses “negative true” logic, the output data was always HIGH.) The MUX and DEMUX share the same 4-bit address as shown to communicate which data channel is active. As before, the address code will be selected using a counter (7493). Again, the TIL 311 is used to display this address.

Start by verifying that your MUX works as you would expect. Use the button to select address 5, then use a slow (~1 Hz) TTL pulse train from the function generator to provide a signal that can be easily identified. Check with a DVM or scope that this is alternating between 0V and +5V before connecting it to your circuit! Plug this signal into the correct MUX input pin for the selected address (which pin?) and verify that the signal is being transmitted to the DEMUX input on pin 18. Select a different address and verify that the slow pulse train is no longer being transmitted.

Once you are sure the data is getting to the DEMUX properly, move your pulse train input to a different MUX channel and check the appropriate DEMUX output. Does the data on the DEMUX output selected by the address counter reproduce the MUX input? Do the other (non-selected) inputs influence the output? What is the state of the non-selected inputs (logic HI or LO)? Check several other addresses and note whether data is being properly transmitted from MUX to DEMUX.

2.3 Cleanup

Congratulations, you have built your first non-trivial digital logic circuit. Please be careful when removing the ICs from the breadboards, and always make sure you TURN OFF THE POWER when inserting or removing ICs.
Figure 1: Decoder circuit schematic. Note that pin 12 of the 74154 is not an output.
Figure 2: Schematic for serial data transmission via MUX/DEMUX.
DM5490/DM7490A, DM7493A
Decade and Binary Counters

General Description
Each of these monolithic counters contains four master-slave flip-flops and additional gating to provide a divide-by-two counter and a three-stage binary counter for which the count cycle length is divide-by-five for the 90A and divide-by-eight for the 93A.

All of these counters have a gated zero reset and the 90A also has gated set-to-nine inputs for use in BCD nine’s complement applications.

To use their maximum count length (decade or four-bit binary), the B input is connected to the QA output. The input count pulses are applied to input A and the outputs are as described in the appropriate truth table. A symmetrical divide-by-ten count can be obtained from the 90A counters by connecting the QD output to the A input and applying the input count to the B input which gives a divide-by-ten square wave at output QA.

Features
- Typical power dissipation
  - 90A 145 mW
  - 93A 130 mW
- Count frequency 42 MHz

Connection Diagrams

Dual-In-Line Package

Order Number DM5490J, DM5490W or DM7490AN
See NS Package Number J14A, N14A or W14B

Dual-In-Line Package

Order Number DM7493AN
See NS Package Number N14A

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4-to-16 line decoder/demultiplexer 74HC/HCT154

PIN DESCRIPTION

<table>
<thead>
<tr>
<th>PIN NO.</th>
<th>SYMBOL</th>
<th>NAME AND FUNCTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 13, 14, 15, 16, 17</td>
<td>$Y_0$ to $Y_{15}$</td>
<td>outputs (active LOW)</td>
</tr>
<tr>
<td>18, 19</td>
<td>$E_0, E_1$</td>
<td>enable inputs (active LOW)</td>
</tr>
<tr>
<td>12</td>
<td>GND</td>
<td>ground (0 V)</td>
</tr>
<tr>
<td>23, 22, 21, 20</td>
<td>$A_0$ to $A_3$</td>
<td>address inputs</td>
</tr>
<tr>
<td>24</td>
<td>$V_{CC}$</td>
<td>positive supply voltage</td>
</tr>
</tbody>
</table>

Fig.1 Pin configuration.
Fig.2 Logic symbol.
Fig.3 IEC logic symbol.
Fig.4 Functional diagram.
54150/DM54150/DM74150, 54151A/DM54151A/DM74151A Data Selectors/Multiplexers

General Description
These data selectors/multiplexers contain full on-chip decoding to select the desired data source. The 150 selects one-of-sixteen data sources; the 151A selects one-of-eight data sources. The 150 and 151A have a strobe input which must be at a low logic level to enable these devices. A high level at the strobe forces the W output high and the Y output (as applicable) low.

The 151A features complementary W and Y outputs, whereas the 150 has an inverted (W) output only.

The 151A incorporates address buffers which have symmetrical propagation delay times through the complementary paths. This reduces the possibility of transients occurring at the output(s) due to changes made at the select inputs, even when the 151A outputs are enabled (i.e., strobe low).

Features
- 150 selects one-of-sixteen data lines
- 151A selects one-of-eight data lines
- Performs parallel-to-serial conversion
- Permits multiplexing from N lines to one line
- Also for use as Boolean function generator
- Typical average propagation delay time, data input to W output
  - 150: 11 ns
  - 151A: 9 ns
- Typical power dissipation
  - 150: 200 mW
  - 151A: 135 mW
- Alternate Military/Aerospace device (54150, 54151A) is available. Contact a National Semiconductor Sales Office/Distributor for specifications.

Connection Diagrams

Dual-In-Line Package

Connection Diagram for 54150/DM54150/DM74150

Connection Diagram for 54151A/DM54151A/DM74151A

Order Number 54150DGMB, 54150FMQB, DM54150J or DM74150N
See NS Package Number J24A, N24A or W24C

Order Number 54151ADMQB, 54151AFMQB, DM54151AJ, DM54151AW or DM74151AN
See NS Package Number J16A, N16E or W16A