6.1 Introduction

Parts List:

- ICs: 311, AD557, 74LS503, 74HCT574
- Resistors: 470 Ω, 1 kΩ, 10 kΩ, 4.7 MΩ, 1 kΩ potentiometer
- Capacitors: 0.1 μF
- Other: LED (red)

Preamble

In this lab, we have to be careful with the ICs, since one of them is delicate and expensive (AD557). Thus note the special policies for this lab:

- **You must** “check out/check in” the AD557 with Rudy or me before beginning your work. We will test it beforehand to make sure it is working, and retest it afterwards to make sure this is still the case.

- You are responsible for the well-being of the chips while they are in your possession.

- To protect the chips, make all circuit connections with the proto-board power **off**, and ask one of us to double-check your wiring **before** powering on the circuit. Thus, you should work on this only during **regular lab times** unless you make arrangements with one of us to be available.

Note that the AD557’s are mounted in sockets to help reduce wear and tear from inserting them in and removing them from breadboards. You should leave them this way (insert the chip/socket combination right into the breadboard), and remember to still always use a chip-puller tool to remove the chips.

The other detail is that the 74LS503 is out of production and difficult to come by. Thus, we will use an emulator IC for the ’503, designed by Prof. Steck using a programmable logic device—make sure to use the correct pinout diagram for the emulator and not for the original IC. The pinout diagram for the emulator is included in this handout, just before the original data sheet.

Because this lab is a bit long and our supply of AD557s is a bit limited, you should work with a partner in this lab.

6.2 Introduction

In this lab, you will build an 8-bit analog-to-digital converter (ADC) using the successive-approximation technique. The overall scheme is shown in Figure 1 below. The input is compared (using the LM311) to the most recent digital estimate, which is converted to analog using the AD557 digital to analog (D/A) converter (DAC). The 74LS503 successive approximation register (SAR) carries out the binary-search algorithm and performs all necessary control functions. At the end of the conversion process, the result is latched by the 74574 8-bit register.

Typically, all components shown in the figure are integrated into a single ADC IC, which does not allow you to examine the internal workings of the device, as we will do in this lab.
6.3 DAC Checkout

First, we need to make sure we understand how the DAC works. We will connect the DAC as shown in Figure 2. (See also the pages from the attached AD557 data sheet.) Note that only pin 11 is connected to +5 V. With the output connected in this way, the analog output has the range 0 to 2.55 V, corresponding to 10 mV per bit for the 8-bit digital input of 0 to $2^8 - 1$. The ceramic capacitor may be necessary to eliminate runaway oscillation of the output. The CS and CE control functions won’t be needed for this lab and should be connected to ground, as shown. **Note that for proper operation, the power and ground connections to pins 9-13 should always be connected as shown. These connections will be omitted in the rest of the schematics in this lab to keep the clutter down, but make sure they’re there; otherwise the chip will likely suffer damage.** Pins 14 and 15 should also remain shorted to pin 16 in the rest of the circuits in the lab; otherwise the DAC output won’t be correct.

6.3.1 Output Voltages

While reading $V_{out}$ on a DVM, check out the effect of the input lines. Connect the 8 input pins to the DIP switches on the trainer board. These switches assert either +5 V or ground, and since any disconnected inputs will float high, it is important to provide a well defined voltage for all inputs. Explain briefly what the DAC should do. Test this by playing with the DIP switch settings. What output does an input of $11111111_2$
or 10000000₂ give? How about 00000000₂ and 00000001₂? Are these correct based on what you expect? If you do not see what you expect, check in with your TA. Your AD557 chip may be damaged.

6.3.2 Resolution and Output Noise

Look at $V_{out}$ on the oscilloscope. How does the difference between 00000000₂ and 00000001₂ compare to the level of noise? Qualitatively, what kind of frequency spectrum does the noise have? (That is, is there some specific frequency that seems to be most noticeable?) For this exercise, make sure to attach the ground clip of the scope probe as close as possible to the AD557 ground, otherwise you may get excessive noise pickup.

6.4 A/D in Slow Motion

Now we can connect the successive approximation register (SAR) and voltage comparator to make our first ADC circuit. The detailed connection scheme is shown in Figure 3. Make sure you keep the power, ground, and output connections from the previous AD557 schematic.

We will begin by evaluating this ADC in slow motion, clocking it by hand. The pin connections for the LM311 comparator are shown in Figure 4. We should not need to use the balance adjustment (pins 5 and 6) for this lab. For this lab, use $V_{CC} \approx +6$ V and $V_{EE} \approx -6$ V. (If you notice the output of the 311 bouncing around a lot, try adding some capacitance between pins 3 and 7 – check with the TA.) The 1 kΩ pull-up resistor to +5 V is required to set the logic HIGH level to +5 V. The logic LOW is determined by the connection to pin 1 of the 311: in this case we want 0 V.

To enable hand-clocking of the SAR, use the prototype board debounced switches connected as shown in Figure 5. The connection for the clock is shown on the left, and the connection for $\overline{START} = \overline{S}$ is on the right.

Finally, provide an adjustable DC analog input by connecting the analog input (at the 10kΩ resistor) to the variable resistor of the prototype board, as shown in Figure 6.
Figure 4: Connections for the LM311 comparator. For this lab use $V_{CC} \approx +6 \, V$ and $V_{EE} \approx -6 \, V$. We should not need to use the balance adjustment (pins 5 and 6) here.

Figure 5: Debounced switch connections. To ensure good logic levels, provide pull-up resistors as shown. Test your buttons using one of the LEDs on the trainer board, as some of them have gone bad.

Figure 6: Potentiometer connection to provide an adjustable analog voltage.
6.4.1 Conversion Completed

Connect the 8 proto-board LEDs to the SAR outputs Q0–Q7 so that you can directly view the current digital estimate. Finally, we need to see when the SAR has completed its conversion cycle: The \( \overline{CC} \) pin goes LOW when the cycle is complete. Connect a separate red LED with a current-limiting resistor \( \approx 470 \, \Omega \), as shown above in the schematic with the SAR. The LED should be off during conversion and turn on when conversion is complete. Finally, note that pin 4 of the (emulated) SAR is a “chip enable” \( \overline{E} \); this must be grounded.

6.4.2 Binary Search

The SAR is a “synchronous” device, so it will start conversion only when the \( \overline{S} \) signal is accompanied by a clock pulse. Give your device some DC input voltage (measure with a DVM or scope). Now start the conversion and watch the analog estimate (output of DAC) with a DVM and the digital estimate (LEDs) while issuing additional clock pulses by hand. The binary search pattern should be evident.

How many clock pulses occur from start to end of conversion? Carefully measure 6 input analog values including zero and full scale, and fill out a table with the following 5 headings:

<table>
<thead>
<tr>
<th>( V_{\text{in}} )</th>
<th>( V_{\text{DAC}} )</th>
<th>Expected Digital Out</th>
<th>Measured Digital Out (LEDs)</th>
<th>Ratio (Measured/Expected)</th>
</tr>
</thead>
</table>

Is the response linear? Make a plot of the ratio (digital output / expected) vs. \( V_{\text{in}} \). Estimate the maximum nonlinearity over the full input range. Is it consistent with \( \pm \text{LSB}/2 \)? Is there an offset?

6.5 Normal-Speed Checkout

Set up continuous-cycling operation by replacing the SAR start \( \overline{S} \) button with a connection from \( \overline{CC} \). That is, directly connect pin 2 to pin 14. Replace the clock button input with the TTL output from a function generator. Run the clock frequency somewhere in the range 10 kHz to 100 kHz.

6.5.1 Watching the Conversion Process

Connect a scope probe to the DAC output. Trigger the scope on \( \overline{CC} \). Now watch the conversion process on the scope. Vary the analog input and watch your ADC converge to the input value. Compare what you see to Fig. 9.52A of Horowitz and Hill (attached).

6.5.2 High-Frequency Conversion

Now, replace your clock with the TTL output of one of the 2-MHz function generators in the lab. Watch the conversion process while increasing the clock frequency. You will probably notice a lot of parasitic capacitive coupling at the highest frequencies. But beyond this noise, does the final ADC value remain steady with increasing frequency? Is there a breakdown frequency, where the conversion no longer works properly?

6.5.3 Binary-Search Tree

Now we will make a pretty display. Use a clock with frequency of a few tens of kHz. Using an external function generator, give your ADC an input consisting of a triangle wave of frequency \( \sim 100 \, \text{Hz} \) and amplitude which spans the range of your ADC. Set up the scope as before. You should now see the entire binary search pattern on the scope, as your ADC attempts to converge to all possible input values. By carefully tuning the frequencies of triangle and clock, it is possible to get a (nearly) stationary pattern. Note that this works well on analog scopes; if you are using a digital scope, try putting it in persistence mode if it has one. Compare with Horowitz and Hill Fig. 9.52B (attached). Make a hardcopy of your trace using a cell phone camera or ask the TA to help. Include this in your report. You might also want to post this to your favorite social media...
6.6 Completing the ADC

Note: to save time, since this is a long lab, you may skip this last section if you run out of time in the lab; however, you should still read through and describe in your logbook how you would have completed the circuit with a register. This includes answering the questions about Logic X below.

Any real ADC will have a digital output that is latched and stored at the end of the conversion cycle. This will be done using the 8-bit D-type positive-edge-triggered register (74HCT574) shown in Figure 7. Connect up the 74HCT574 as shown, connecting the LEDs to its outputs.

![Partial schematic showing final output register.](image)

6.6.1 Logic X

We need to provide a clock signal to latch the output at the end of the conversion cycle. A clear candidate for this signal would be the rising edge of the SAR signal as it returns from LOW to HIGH. Try using this. Vary the analog input and watch the LEDs. You should find that one of the LEDs never lights up. Which one? The reason for this can be seen from the timing diagram shown below. The rising edge of SAR occurs too late, after the next cycle has begun. Similarly, the falling edge of SAR is too early. In this case, the LSB would never be set.

By examining the timing diagram in Figure 8, can you find a single digital gate that provides the pulse we want, labeled “X” in the schematic above? Connect this up and draw your “logic X” box. You may need to consult one of the TTL books in the lab to get the right IC and connection scheme. With this connection, verify that all digital bits can now be latched.

![Timing for output register latching.](image)
DACPORT Low Cost, Complete μP-Compatible 8-Bit DAC

**FEATURES**
- Complete 8-Bit DAC
- Voltage Output: 0 V to 2.56 V
- Internal Precision Band-Gap Reference
- Single-Supply Operation: 5 V (±10%)
- Full Microprocessor Interface
- Fast: 1 μs Voltage Settling to ±1/2 LSB
- Low Power: 75 mW
- No User Trims Required
- Guaranteed Monotonic Over Temperature
- All Errors Specified T_MIN to T_MAX
- Small 16-Lead DIP or 20-Lead PLCC Package
- Low Cost

**PRODUCT DESCRIPTION**

The AD557 DACPORT® is a complete voltage-output 8-bit digital-to-analog converter, including output amplifier, full microprocessor interface and precision voltage reference on a single monolithic chip. No external components or trims are required to interface, with full accuracy, an 8-bit data bus to an analog system.

The low cost and versatility of the AD557 DACPORT are the result of continued development in monolithic bipolar technologies.

The complete microprocessor interface and control logic is implemented with integrated injection logic (I^2L), an extremely dense and low-power logic structure that is process-compatible with linear bipolar fabrication. The internal precision voltage reference is the patented low-voltage band-gap circuit which permits full-accuracy performance on a single 5 V power supply. Thin-film silicon-chromium resistors provide the stability required for guaranteed monotonic operation over the entire operating temperature range, while laser-wafer trimming of these thin-film resistors permits absolute calibration at the factory to within ±2.5 LSB; thus, no user-trims for gain or offset are required. A new circuit design provides voltage settling to ±1/2 LSB for a full-scale step in 800 ns.

The AD557 is available in two package configurations. The AD557JN is packaged in a 16-lead plastic, 0.3"-wide DIP. For surface mount applications, the AD557JP is packaged in a 20-lead JEDEC-standard PLCC. Both versions are specified over the operating temperature range of 0°C to 70°C.

**PRODUCT HIGHLIGHTS**

1. The 8-bit I^2L input register and fully microprocessor-compatible control logic allow the AD557 to be directly connected to 8- or 16-bit data buses and operated with standard control signals. The latch may be disabled for direct DAC interfacing.

2. The laser-trimmed on-chip SiCr thin-film resistors are calibrated for absolute accuracy and linearity at the factory. Therefore, no user trims are necessary for full rated accuracy over the operating temperature range.

3. The inclusion of a precision low-voltage band-gap reference eliminates the need to specify and apply a separate reference source.

4. The AD557 is designed and specified to operate from a single 4.5 V to 5.5 V power supply.

5. Low digital input currents, 100 μA max, minimize bus loading. Input thresholds are TTL/low voltage CMOS compatible.

6. The single-chip, low power I^2L design of the AD557 is inherently more reliable than hybrid multichip or conventional single-chip bipolar designs.

DACPORT is a registered trademark of Analog Devices, Inc.

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**REV. B**

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**AD557—SPECIFICATIONS (\( @ T_A = 25^\circ C, V_{CC} = 5 \) V unless otherwise noted)**

<table>
<thead>
<tr>
<th>Model</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>RESOLUTION</td>
<td>8</td>
<td></td>
<td></td>
<td>Bits</td>
</tr>
<tr>
<td>RELATIVE ACCURACY</td>
<td>±1/2</td>
<td>1</td>
<td></td>
<td>LSB</td>
</tr>
<tr>
<td>0°C to 70°C</td>
<td></td>
<td></td>
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<tr>
<td>OUTPUT Ranges</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Current Source</td>
<td>5</td>
<td></td>
<td></td>
<td>mAh</td>
</tr>
<tr>
<td>Sink</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Pull-Down to Ground</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

| Range          | 0 to 2.56 |     |     | V    |
| Current Source | 5         |     |     | mAh  |
| Sink          | 5         |     |     | mAh  |

**OUTPUT SETTLING TIME**

- 0.8 \( \mu \)s
- 1.5 \( \mu \)s

**FULL-SCALE ACCURACY**

- @ 25°C: ±1.5 ±2.5 LSB
- @ T_MIN to T_MAX: ±2.5 ±4.0 LSB

**ZERO ERROR**

- @ 25°C: ±1 LSB
- @ T_MIN to T_MAX: ±3 LSB

**MONOTONICITY**

- Guaranteed But Not Tested

**DIGITAL INPUTS**

- T_MIN to T_MAX: ±100 µA
- Data Inputs, Voltage
  - Bit On—Logic "1": 2.0 V
  - Bit On—Logic "0": 0 V
- Control Inputs, Voltage
  - On—Logic "1": 2.0 V
  - On—Logic "0": 0 V
- Input Capacitance: 4 pF

**TIMING**

- \( t_W \) Strobe Pulsewidth: 225 ns
- \( t_DH \) Data Hold Time: 10 ns
- \( t_DS \) Data Setup Time: 225 ns
- \( t_{MIN} \) to \( t_{MAX} \)

**POWER SUPPLY**

- Operating Voltage Range (V_{CC})
  - 2.56 V
  - Current (I_{CC}): 15 mA
  - Rejection Ratio: 0.03 %

**POWER DISSIPATION, V_{CC} = 5 V**

- 75 mW
- 125 mW

**OPERATING TEMPERATURE RANGE**

- 0°C to 70°C

**NOTES**

1. Relative Accuracy is defined as the deviation of the code transition points from the ideal transfer point on a straight line from the offset to the full scale of the device. See “Measuring Offset Error” on the AD558 data sheet.
2. Passive pull-down resistance is 2 kΩ.
3. Settling time is specified for a positive-going full-scale step to ±1/2 LSB. Negative-going steps to zero are slower, but can be improved with an external pull-down.
4. The full-scale output voltage is 2.55 V and is guaranteed with a 5 V supply.
5. A monotonic converter has a maximum differential linearity error of ±1 LSB.
6. See Figure 7.

Specifications shown in **boldface** are tested on all production units at electrical test. Specifications subject to change without notice.

**ORDERING GUIDE**

<table>
<thead>
<tr>
<th>Model</th>
<th>Temperature Range</th>
<th>Package Description</th>
<th>Package Option</th>
</tr>
</thead>
<tbody>
<tr>
<td>AD557JN</td>
<td>0°C to 70°C</td>
<td>Plastic DIP</td>
<td>N-16</td>
</tr>
<tr>
<td>AD557JP</td>
<td>0°C to 70°C</td>
<td>Plastic Led Chip Carrier</td>
<td>P-20A</td>
</tr>
</tbody>
</table>

**ABSOLUTE MAXIMUM RATINGS**

- V_{CC} to Ground: 0 V to 18 V
- Digital Inputs (Pins 1–10): 0 V to 7.0 V
- V_{OUT}: Indefinite Short to Ground
- Momentary Short to V_{CC}

**Storage Temperature Range**

- N/P (Plastic) Packages: –25°C to +100°C
- Lead Temperature (Soldering, 10 sec): 300°C

**Thermal Resistance**

- Junction to Ambient/Junction to Case

**PIN CONFIGURATIONS**

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**REV. B**
This document briefly describes the implementation of an emulator, based on the ATF750C CPLD, of the 74LS503 successive-approximation register, formerly available from Fairchild Semiconductor. More details about chip operation are available in Fairchild’s original data sheets for the DM74LS503 and DM74LS502, and more details about this particular emulator can be found online. Files for “burning” the PLD emulator can also be found online.

Schematic symbol (emulator):

Pin diagram compared to original:

---


2http://atomoptics-nas.uoregon.edu/~dsteck/teaching/74503
DM74LS503
8-Bit Successive Approximation Register (with Expansion Control)

General Description
The DM74LS503 register has an active LOW Enable (E) input that is used in cascading two or more packages for longer word lengths. A HIGH signal on E, after a START operation, forces Q7 HIGH and prevents the device from accepting serial data. With the E input of an DM74LS503 connected to the CC output of a preceding (more significant) device, the DM74LS503 will be inhibited until the preceding device is filled, causing its CC output to go LOW. This LOW signal then enables the DM74LS503 to accept the serial data on subsequent clocks.

Features
- Performs serial-to-parallel conversion
- Expansion control for longer words
- Storage and control for successive approximation A to D conversion
- Low power Schottky version of 2503

Ordering Code:

<table>
<thead>
<tr>
<th>Order Number</th>
<th>Package Number</th>
<th>Package Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>DM74LS503N</td>
<td>N16E</td>
<td>16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide</td>
</tr>
</tbody>
</table>

Connection Diagram

Logic Symbol

Pin Descriptions

<table>
<thead>
<tr>
<th>Pin Names</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>D</td>
<td>Serial Data Input</td>
</tr>
<tr>
<td>S</td>
<td>Start Input (Active LOW)</td>
</tr>
<tr>
<td>CP</td>
<td>Clock Pulse Input (Active Rising Edge)</td>
</tr>
<tr>
<td>E</td>
<td>Conversion Enable Input (Active LOW)</td>
</tr>
<tr>
<td>CC</td>
<td>Conversion Complete Output (Active LOW)</td>
</tr>
<tr>
<td>Q0–Q7</td>
<td>Parallel Register Outputs</td>
</tr>
<tr>
<td>Q7</td>
<td>Complement of Q7 Output</td>
</tr>
</tbody>
</table>
A variant on the simple parallel encoder is the so-called half-flash technique, a two-step process in which the input is flash-converted to half the final precision; an internal DAC converts this approximation back to analog, where the difference “error” between it and the input is flash-converted to obtain the least significant bits (Fig. 9.50). This technique yields low-cost converters that are faster than anything else except full flash converters. It is used in inexpensive converters like the 8-bit ADC0820 (National) and AD7820/4/8 (Analog Devices).

Flash encoders are worth considering in waveform digitizing applications even when the conversion rate is relatively slow, because their high speed (or, more precisely, their short aperture interval, during which the comparator outputs are latched) ensures that the input signal is effectively not changing during the conversion. The alternative – the slower converters we'll describe next – usually requires an analog sample-and-hold circuit to freeze the input waveform while conversion is going on.

**Successive approximation**

In this popular technique you try various output codes by feeding them into a D/A converter and comparing the result with the analog input via a comparator (Fig. 9.51). The way it's usually done is to set all bits initially to 0. Then, beginning with the most significant bit, each bit in turn is set provisionally to 1. If the D/A output does not exceed the input signal voltage, the bit is left as a 1; otherwise it is set back to 0. For an n-bit A/D, n such steps are required. What you're doing could be described as a binary search, beginning at the middle. A successive-approximation A/D module has a BEGIN CONVERSION input and a CONVERSION DONE output. The digital output is always provided in parallel format (all bits at once, on n separate output lines) and usually in serial format as well (n successive output bits, MSB first, on a single output line).

In our electronics course the students construct a successive-approximation ADC, complete with DAC, comparator, and control logic. Figure 9.52A shows the

![Figure 9.50. Half-flash ADC.](image-url)
successive outputs from the DAC, along with the eight clock pulses, as the trial analog output converges to the input voltage. Figure 9.52B shows the full 8-bit "tree," a pretty picture you can generate by watching the DAC output while driving the input with a slow ramp that runs over the full analog input range. Successive-approximation A/D converters are relatively accurate and fast,