4 Counters, Registers, and State Machines

We can now apply what we know about basic flip-flops circuit elements to develop new functions: counters and registers. In doing so, we will introduce the “state machine”, a clocked sequential “processor”. We will examine this latter topic in more detail in a few weeks.

4.1 Divide by Two Counter

The edge-triggered D-type flip-flops which we introduced in the previous Section are quite useful and versatile building blocks of sequential logic. A simple application is the divide-by-2 counter shown in Fig. 1, along with the corresponding timing diagram.

![Figure 1: Positive edge-triggered D-type flip-flop connected as divide-by-2 counter.](image)

4.1.1 Using the JK Flip-flop

In Lab 4 you will build an asynchronous (ripple) counter using a sequence of cascaded JK flip-flops, rather than the D-type which is used in our discussion below. For reference, the JK truth table is given in Fig. 2. Note that there is no fundamental advantage to using the JK instead of the D-type, only that the JK, with the additional \( J = K = 1 \) state, makes the divide-by-2 function slightly simpler to implement.

![Figure 2: The JK Flip-flop.](image)
4.2 Asynchronous Counter

Flip-flops can be connected in series, as shown in Fig. 3. The resulting outputs are given in Fig. 4. (Note that labels in these two figures correspond when $A \equiv 2^0$, $B \equiv 2^1$, $C \equiv 2^2$, and $D \equiv 2^3$. Hence, this is a 4-bit counter, with maximum count $2^4 - 1 = 15$. It is clearly possible to expand such a counter to an indefinite number of bits.

While asynchronous counters are easy to assemble, they have serious drawbacks for some applications. In particular, the input must propagate through the entire chain of flip-flops before the correct result is achieved. Eventually, at high input rate, the two ends of the chain, representing the LSB and MSB, can be processing different input pulses entirely. (Perhaps in lab you can see this effect on the oscilloscope with a very high input frequency.) The solution to this is the synchronous counter, which we will discuss below as an example of a state machine.

![Figure 3: Asynchronous (“ripple”) counter made from cascaded D-type flip-flops.](image)

![Figure 4: Waveforms generated by the ripple counter.](image)
4.3 Registers

4.3.1 Basic Register

The figure below represents a 4-bit memory. We can think of it as 4 individual D-type flip-flops. The important point about a data register of this type is that all of the inputs are latched into memory synchronously by a single clock cycle.

![4-bit data register](image)

Figure 5: 4-bit data register.

4.3.2 Shift Registers

The figure below is an example of a 4-bit shift register. These configurations are quite useful, particularly for transforming serial data to parallel, and parallel to serial. In the circuit below, a pulse appearing at “serial in” would be shifted from the output of one flip-flop to the next on each clock cycle. Hence a serial bit pattern at the input (4 bits long in this example) would appear as 4 parallel bits in the outputs $Q_0$–$Q_3$ after 4 clock cycles. This represents the serial-to-parallel case.

![4-bit shift register](image)

Figure 6: 4-bit shift register.

We will discuss several examples of shift registers a few lectures hence.